

# On board computing system for AMS-02 mission

X.Cai for the AMS02 Collaboration

Massachusetts Institute for Technology, Cambridge MA, USA

Presenter: Xudong CAI (Xudong.Cai@cern.ch), swi-cai-xudong-abs1-og15-oral

The AMS data acquisition system is based on a tree structure of data collection modules. At the top level, 4 redundant computers (called MDC, Main DAQ Computer) control the entire system and collect data from the sub-systems. This contribution presents a detailed description of the design and functions of the MDCs.

## 1. The system requirements and hardware design

The architecture of the AMS DAQ system is shown in Fig. 1. Physics data taken by the subdetectors (~300k channels) are collected by two levels of CDDC (Command Distributor and Data Concentrator) modules. Top level CDDC forwards the data to the Main DAQ Computer (MDC), which performs level 3 trigger (software event selection) and data compression, then send the data through ISS interface to the data storage inside the ISS US lab, and eventually downlink to the ground stations. The allocated downlink rate is 2 Mbits/sec, averaged over one orbit. With the expected ~2k Hz peak trigger rate, substantial processing power is needed to reduce the data volume before downlink. In addition, the MDC also perform the house keeping tasks by commanding and collecting data from the USCMs (Universal Slow Control Module), which perform the actual measurements. The house keeping functions include temperature measurements, heater control, high voltage and low voltage setting and monitoring, and magnetic field measurements.

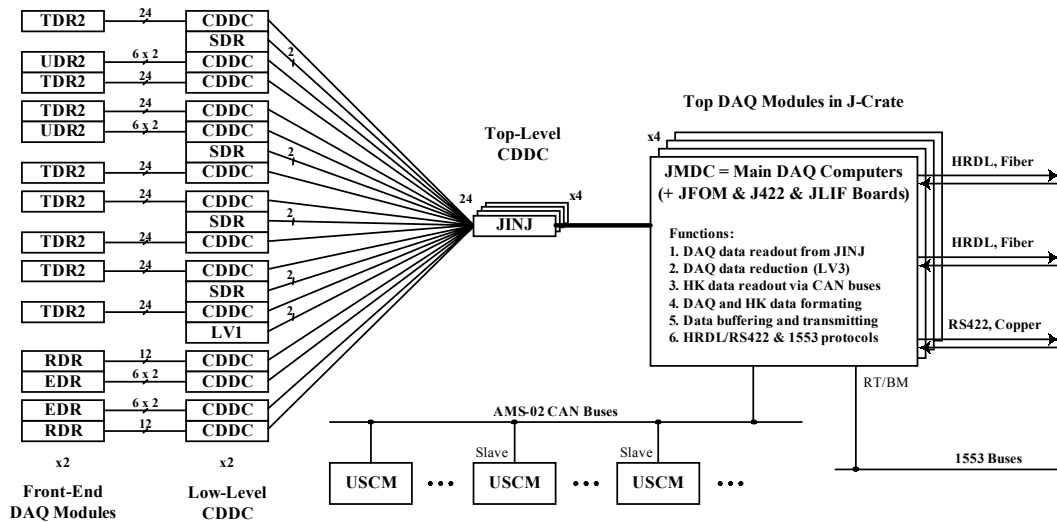


Figure 1. AMS DAQ System

In summary, the top level computer serves the following functions:

- Collecting data from subsystems via AMSWIRE interfaces.
- Event building, level 3 trigger, and temporary storage.
- Performing house keeping functions via a dual-redundant CAN network.
- Interface to International Space Station (ISS) through High Rate Data Link (HRDL) and Low Rate Data Link (LRDL).

Since there will be no maintenance service during the complete AMS mission, the top level computers has to be very reliable. The system is designed with four independent computers (MDC), each capable of fulfill the AMS operation requirements. Each MDC has one single board computer, a memory module, and several interface boards, connected through a dedicated Compact PCI bus. Fig. 2 shows the schematics of the system. The four MDC, together with the interface boards for ISS and the Shuttle, are located in one mechanical crate, called J-Crate. The functionalities of each board in the J-Crate are described in the following.

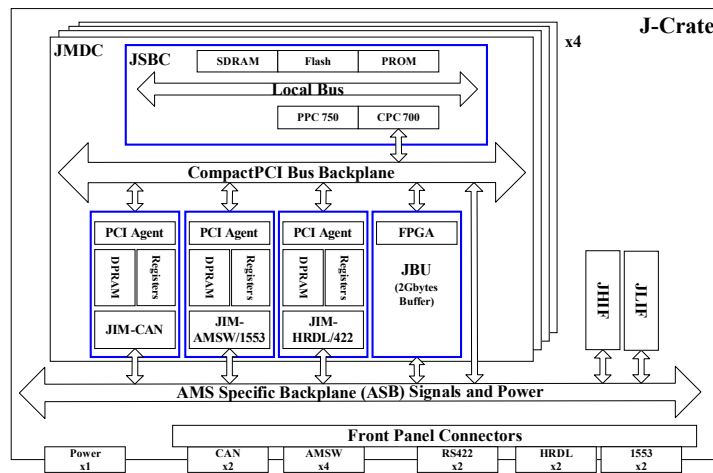


Figure 2. AMS J-Crate Schematics

**The single board computer (SBC)** is the main intelligence unit of the MDC. The core of SBC is a PowerPC 750 CPU running at 400 MHz. CPC700 is used as memory controller and PCI north-bridge to access all other PCI periphery boards. On board memories include 256 Mbytes of SDRAM, 32Mbytes of flash memory for main SBC program, and a radiation hard PROM for boot loader called ROM monitor.

**The buffer memory board (JBU)** is designed with 2 Gbytes of SDRAM which can buffer data corresponding to  $\sim 1.5$  orbit in case of losing downlink communication. The JBU memory is divided into 8 segments, each is powered up independently to reduce power consumption.

**The AMSWIRE/1553 interface board** integrates two functions, AMSWIRE and 1553 interfaces on the same board. The AMSWIRE is a point-to-point serial communication protocol designed for AMS. The AMSWIRE is used to collect data from subsystem and to interconnect the four MDCs. The board consists of two 1553 controllers and 10 AMSWIRE links, 4 for DAQ tree and 6 for inter-connection of four MDCs. Total 256K onboard memories are shared by all AMSWIRE channels.

**The CAN interface board** connects the interface to the two redundant CAN buses. In order to adapt fast SBC and slow CAN controllers, we introduce a microcontroller 8051 and 256K memory between them to control the CAN communication.

**The HRDL/422 interface board** connects MDC to the main science data path to ISS (HRDL) or to space shuttle (RS422). Both communication modes use the frames formatted in NASA standard. The decoding and encoding works are done by SBC. The TX and RX share the 256K memory buffers.

**The JHIF board** is used to make a single connection from four MDCs to NASA equipments for HRDL and RS422 links. It acts as a concentrator. Two redundant parts for HRDL link which is the main path to send science data to ISS. Only one of them is power at a time.

**The JLIF board** concentrates the low rate signals from the four MDC computers similar to the JHIF board.

**The J-Crate backplane** (called JBP) is used to hold all the boards in the J-crate. The MDC computer boards conform to the 6U compact PCI form factor. The JBP has four independent compact PCI segments, holding the 4 MDC computers. In the cPCI segments, the lower two cPCI connectors (P1 and P2) are standard PCI signals, while the upper two connectors (P4, P5) are used for AMS specific signals.

## 2. Software and operation

The software for the SBCs contains two major software systems. The first is the ROM Monitor stored in the radiation hard PROM. The second is the main DAQ program, which is normally stored in the onboard flash memory.

### 2.1 The ROM Monitor

On boot, the SBCs load automatically the ROM Monitor program from the PROM. The main tasks of ROM monitor are to initialize the SBC hardware and to start main DAQ software. The hardware will indicate the boot source which can be due to Watchdog timer timeout, CPU exception, external boot command, or simply power up.

In case of the Watchdog timer timeout or CPU exception, the ROM monitor will reload the main DAQ program from the flash memory, and then execute it with default parameters. In other cases, further commands are needed from the ground. ROM monitor has full support of communication with ISS and space shuttle.

### 2.2 The main DAQ software

The normal operations of the SBCs are quite complicated. The software is based on RedHat eCos, a simple embedded operating system. The operating system will support device driver and system calls.

The functions are programmed as tasks and running in parallel. Each task is divided into states and managed by state machine. Any state should last less than 500 $\mu$ s. All tasks are managed by a single scheduler. The data exchange between tasks is using a unified block format, called AMS block. The full memory space is shared by all tasks.

### 2.3 The AMS application tasks

The AMS applications are separated into the following four categories:

- System tasks: including the communication servers for the HRDL, LRDL, CAN, and AMSWIRE interfaces, as well as the display server and the command handler.
- DAQ tasks: control the level-1 trigger module, read science data from CDDC, build the event, and perform level-3 event selection.
- Manual tasks: include various calibration jobs, which are initiated by direct commands, as well as special tasks like uploading new programs.
- House keeping tasks: control and monitor (a) the gas system for the Transition Radiation Detector, (b) the Tracker thermal control, (c) the Magnetic field, (d) the power system, and (e) the temperature sensor network.

## 3. Space qualification and tests

The development of the J-Crate went through 3 stages. The engineering model was made with commercial components and with FPGA for easy diagnostic and corrections. Once the functionality was proved, qualification model was built with flight components. The qualification model went through standard AMS space qualification procedure. The production and qualification procedures are shown in Fig. 3. A few iterations went through due to mistakes found during qualification procedure. Flight modules are built

