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Research Article

Understanding the Resistive Switching Phenomena of Stacked Al/Al_2O_3/Al Thin Films from the Dynamics of Conductive Filaments

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We present the resistive switching characteristics of Metal-Insulator-Metal (MIM) devices based on amorphous Al_2O_3 which is deposited by Atomic Layer Deposition (ALD). A maximum processing temperature for this memory device is 300°C, making it ideal for Back-End-of-Line (BEOL) processing. Although some variations in the forming, set, and reset voltages (V_{FORM}, V_{SET}, and V_{RESET}) are obtained for many of the measured MIM devices (mainly due to roughness variations of the MIM interfaces as observed after atomic-force microscopy analysis), the *memristor* effect has been obtained after cyclic *I-V* measurements. These resistive transitions in the metal oxide occur for both *bipolar* and *unipolar* conditions, while the I_{OFF}/I_{ON} ratio is around 4–6 orders of magnitude and is formed at gate voltages of $Vg < 4$ V. In unipolar mode, a gradual reduction in V_{SET} is observed and is related to combined (a) incomplete dissolution of conductive filaments (made of oxygen vacancies and metal ions) which leaves some residuals and (b) thickening of chemically reduced Al_2O_3 during localized Joule heating. This is important because, by analyzing the macroscopic resistive switching behavior of this MIM structure, we could indirectly relate it to microscopic and/or nanoscopic phenomena responsible for the physical mechanism upon which most of these devices operate.

1. Introduction

Since the invention and experimental demonstration of the *memristor* (an integrated device with *memory-resistance* properties, able to correlate electric charge to magnetic flux *q-φ* [1]), several materials in the form of thin dielectric films or solid electrolytes have been tested for these emergent nonvolatile memory devices in order to produce reliable and reversible switching cycles of the resistive state of the oxide. Thin film based materials able to switch from a high resistance state (HRS/OFF) to a low resistance state (LRS/ON) and vice versa are responsible for the typical *"pinched hysteresis loops,"* which are observed during cyclic current-voltage (*I-V*) measurements of these devices. This has contributed to the development of important applications like nonlinear circuits, chaotic systems, highly dense neural networks, and even neuromorphic computing, where the diffusive dynamics of memristors can be used as synaptic emulators. Nevertheless, all these highly dynamic applications exploiting the memristor effect do so without considering complex microscopic and nanoscopic phenomena, mainly related to the evolution and migration dynamics of atomic elements within the integrated device. Recently, several Metal-Insulator-Metal structures have shown the ability to switch between these two resistive states (HRS ↔ LRS) after promoting resistive switching phenomena (by forming/dissolving conductive filamentary paths in mostly binary oxides) or ion migration mechanisms (by cation or anion species in solid electrolytes) during high electrical stress of the devices [1, 2]. In this sense, Resistive switching Random Access Memory (ReRAM) devices have attracted considerable attention in the recent years due to their superior characteristics for nonvolatile data storage. Some of these advantages are a simple memory structure (usually composed of MIM stacks), deep scalability, ultralow power consumption, fast write/erase speed, and long retention times [3]. Also, even though the precise physics behind

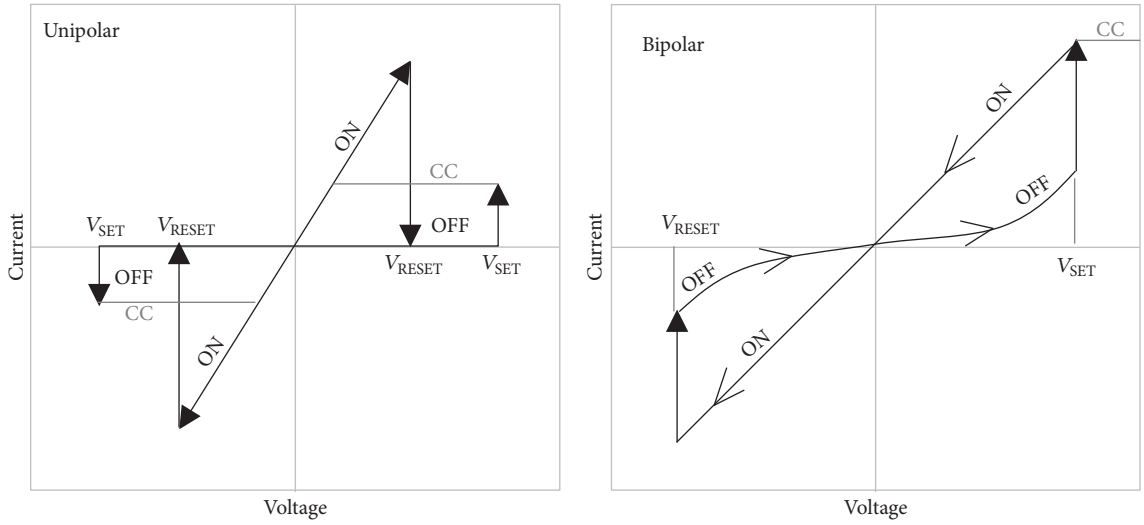


FIGURE 1: $I-V$ diagrams showing the (a) unipolar and (b) bipolar operation modes for ReRAM devices where no dependence of the *"pinched hysteresis loops"* to frequency is involved (DC conditions). The unipolar mode is able to promote resistive switching using a positive or negative polarity with $V_{SET} > V_{RESET}$ and $CC_{SET} < CC_{RESET}$.

the operation mechanism is still not fully understood, by using resistive switching and/or ion migration phenomena, there have been some advances in which, for many cases, single and/or multiple filamentary conduction paths can be formed or dissolved in the oxide, thus connecting or disconnecting both metal electrodes and, therefore, giving origin to both LRS and HRS [4, 5]. This is important because a better understanding of the resistive switching phenomena could enable enhanced nonlinear applications like the ones previously described, while also providing better modeling tools for nonlinear devices and systems. ReRAM switching modes can be classified into two groups: unipolar switching and bipolar switching. In unipolar mode, the resistive switching transitions (HRS $\leftrightarrow$ LRS) of the oxide layer are obtained using the same polarity but different magnitudes of applied bias (while limiting the gate current at two current compliance levels). In bipolar mode, these transitions are obtained using different polarities of applied bias so that typical hysteresis loops in the I-V characteristics (*Lissajous* curves) are observed [3, 5]. In any case, these resistive switching transitions require specific voltages so that V_{SET} and V_{RESET} would promote HRS $\rightarrow$ LRS (ON) and HRS $\leftarrow$ LRS (OFF) transitions, respectively (see Figures 1(a)-1(b)).

Depending on the MIM structure, an additional forming voltage V_{FORM} is necessary in order to force the initial HRS $\rightarrow$ LRS transition and, generally, $V_{FORM} > V_{SET} > V_{RESET}$. It is important to consider that, for any operation mode, a limit in the current flowing through the MIM device should be established in order to prevent permanent oxide breakdown and, therefore, losing the memory effect. In the unipolar mode, two different current limits must be used so that during the creation of a conductive path/filament by V_{SET} a low current compliance limit CC_{SET} would enable a controlled formation of these conductive paths, while a higher current compliance limit CC_{RESET} would be required for the dissolution of this conductive path/filament by V_{RESET} (much like the breakdown of a *fuse* after passing a large current density through it). Usually, more reproducible characterization of ReRAM devices based on MIM structures would require that $V_{FORM} > V_{SET} > V_{RESET}$ and $CC_{RESET} > CC_{SET}$ and doing so by also using specific time-dependent waveforms as polarization sources so that the time-dependent properties of these devices could also be extracted (like the well-known poor frequency dependence of experimental memristors, where the total area of the *pinched hysteresis loops* decreases with the frequency of applied bias). On the other hand, it is known that, during the reset process in the unipolar switching mode, a large current flow (needed to dissolve an already formed conductive filament (CF)) would produce localized Joule heating at this conductive filament which, in turn, could lead to its partial dissolution and, therefore, to a large amount of residuals around it (oxygen vacancies and/or metal ions) [6, 7]. The amount and type of these residuals are largely dependent on the CC levels as well as the velocity during the voltage sweeps needed for the cyclic HRS $\leftrightarrow$ LRS transitions. The residual combination of metal atoms/complexes/compounds within the remaining oxide could contribute to higher leakage currents as well as electrical instabilities (like charge trapping-detrapping events or a gradual reduction in V_{SET}) of ReRAM devices upon more switching cycles, leading to narrowing of the resistive window and, thus, lower endurance. Here, we monitor the gradual reduction in V_{SET} after the 5 initial switching cycles of an $Al/Al_2O_3/Al$ structure (unipolar operation) and we relate this reduction of V_{SET} to residuals of aluminum ions (during partial dissolution of the conductive filament by a large current flow) which act as trap centers that lower the energy barrier of Al_2O_3 while decreasing the set

voltage (25th International Conference on Amorphous and Nanocrystalline Semiconductors).

2. Materials and Methods

For MIM device fabrication, stacked $Al/Al_2O_3/Al$ thin films were sequentially deposited on previously cleaned Corning glass slides and standard photolithography steps were used for gate pattern definition, while the whole stack is finally annealed in N_2 at 300°C. Initially, all glass slides were cleaned by sequential immersion in trichloroethylene (TCE) and acetone (10/10 min) within an ultrasonic vibrator. This is followed by rinsing in deionized water (DI water) by 10 min and the slides are gently dried using an ultrahigh purity N_2 blow. Aluminum is used as bottom and top electrode (BE/TE) for the MIM device. The BE/TE consist of aluminum layers each with 500 nm in physical thickness and they were deposited by E-beam evaporation (Temescal BJD-1800 from Edwards) under ultrahigh vacuum conditions using a deposition rate of 1-2 Å/sec. Al_2O_3 with 20 or 10 nm in thickness were deposited on the BE by thermal ALD at 250°C (Savannah S100 from Cambridge NanoTech) using H_2O and Trimethylaluminum (TMA) as chemical precursors for the oxygen and aluminum elements of Al_2O_3. Also, a thinner Al_2O_3 = 6 nm was used in Metal-Insulator-Semiconductor (MIS) structures in order to confirm the high electrical quality of this metal oxide via *I-V* and *C-V* measurements. The ALD process was performed at 250°C/200 mTorr of temperature/pressure for all 200, 100, or 60 deposition cycles of Al_2O_3 deposition. All these samples were quickly introduced into the e-beam evaporator after ALD of Al_2O_3. There, the evaporation chamber was vacuumed down to 1×10^{-7} Torr in order to minimize the exposure time of the Al_2O_3 surfaces to atmospheric oxygen or any other contaminant of the clean room. Standard photolithography steps followed after complete metallization of these MIM devices. For this, all samples were covered with positive photoresist using standard spinning/baking conditions and exposed to an UV system (Karl Suss MA6) in order to transfer gate patterns to the TE. Gate capacitor areas of 36×10^{-6} cm^2 and 64×10^{-6} cm^2 were used for the MIS and MIM devices, respectively. After gate pattern definition, only the $Al/Al_2O_3/Al/Glass$ (MIM) structures were annealed in pure N_2 (99.999% purity) at 300°C in order to promote densification of Al_2O_3 along with interfacial layer development of this metal oxide with BE/TE (nonstoichiometric Al_xO_y interfacial layers are expected). The complete fabrication procedure is very simple (see Figure 2), while the maximum processing temperature is 300°C. A low thermal budget in the processing of these devices makes them ideal for their integration in the BEOL stages of an integrated circuit, thus further increasing the integration density of memory devices.

3. Results and Discussion

Given the thin physical thickness for Al_2O_3 used in the MIM structures (20 and 10 nm), we have electrically characterized MIS devices in which an even thinner Al_2O_3 = 6 nm has been deposited on silicon by using the same ALD conditions (without thermal annealing). Therefore, by using a silicon surface with very low atomic surface roughness (as compared to a metallic bottom electrode), we are able to assess the intrinsic electrical quality of Al_2O_3. Figures 3(a)-3(b) show the *I-V* and *C-V* characteristics of several $Al/Al_2O_3/n\text{-}Si$ MIS devices in which good uniformity is observed after measuring at least 15 MIS devices for each data set. The *I-V* data (normalized to gate area and oxide thickness) show a high electric field required for oxide breakdown (Ebkd = 7.1 MV/cm) (under accumulation or substrate injection condition), while the resistivity window before and after hard breakdown can be as high as 10 orders of magnitude (for $Eg \leq 2$ MV/cm). The *C-V* data, on the other hand, show a large hysteresis window *H* (measured at flat-band voltage) which is characteristic of a bad Al_2O_3/Si interface, so that several defects (from a large density of dangling bonds to chemical reduction of Al_2O_3 into $AlSi_xO_y$ silicates) would promote higher densities of charge trapping.

Also, moderate capacitance in accumulation turns into a dielectric constant of $k \sim 6$, a relatively low value compared to what is expected for bulk Al_2O_3 ($k \sim 9$) and yet the good uniformity in the *C-V* data is again observed for all measured MIS devices. For the MIM structures, we could expect some deviations from *I-V* data in particular, since large defects are found at the interfaces of Al_2O_3 with both the bottom and top metallic electrodes.

In order to show the cyclic resistive switching characteristics of the metal oxide film, thicker Al_2O_3 = 20 nm (deposited by ALD with the same conditions) was used in an $Al/Al_2O_3/Al/Glass$ stacked structure and electrically characterized before and after the final thermal treatment applied to the device. Figures 4(a)-4(b) show the resistive switching characteristics (in unipolar mode) of this structure. Even though the gate current levels are increased for the annealed sample (especially during the HRS condition), we notice that different current compliance levels are needed for both samples whenever we promote a transition from the HRS to the LRS condition and vice versa. For this thicker Al_2O_3, the limit in CC_{SET} is set to 100 μA, whereas CC_{RESET} = 100 mA; both are large current densities flowing through the oxide layer and that would increase the chances for leaving large amount of residuals (after the RESET condition which produce localized Joule heating in the previously formed conductive filament) in the form of a high density of oxygen vacancies (neutral or charged) and/or metal ions. We also observe that some electrical instabilities in the gate current *I*g do occur after the initial resistive switching cycles, where the as-deposited and annealed samples produce 8 and 16 cycles (HRS $\leftrightarrow$ LRS transitions), respectively. These electrical instabilities are due to charge trapping-detrapping events that, later, are related to conduction mechanisms, where trap-energy levels are responsible for these phenomena.

The conduction mechanisms initially considered for modeling these gate tunneling currents were Ohmic Conduction (OC), Thermionic Emission (TE), Space-Charge Limited Current (SCLC), Trap-Assisted Tunneling (TAT), Poole-Frenkel (PF), and Fowler-Nordheim (FN). After linear fitting of the experimental *I-V* data (only for the HRS condition just before oxide breakdown or conductive filament formation),

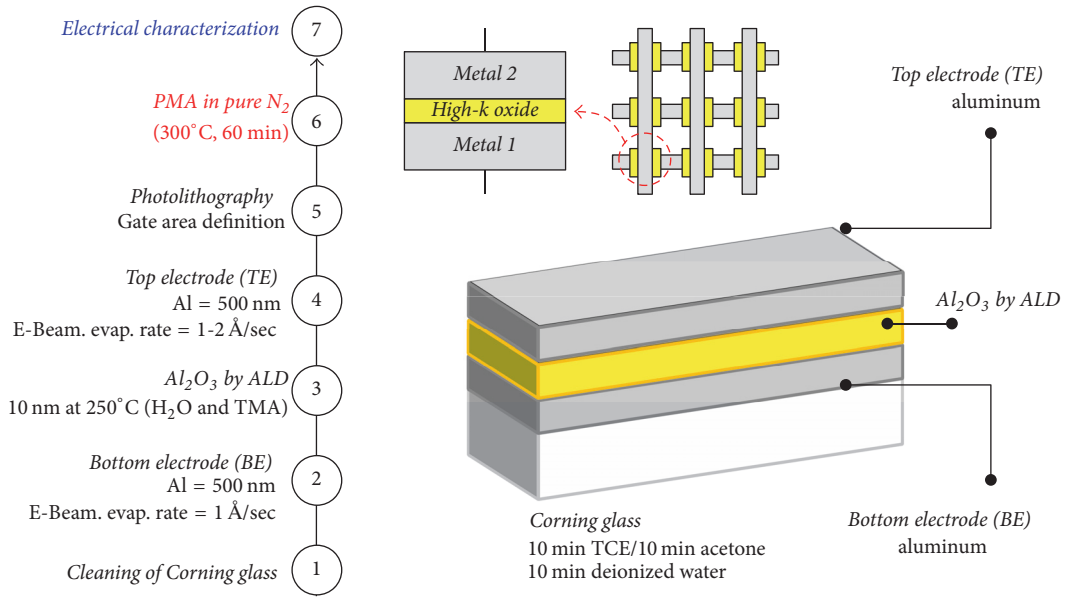
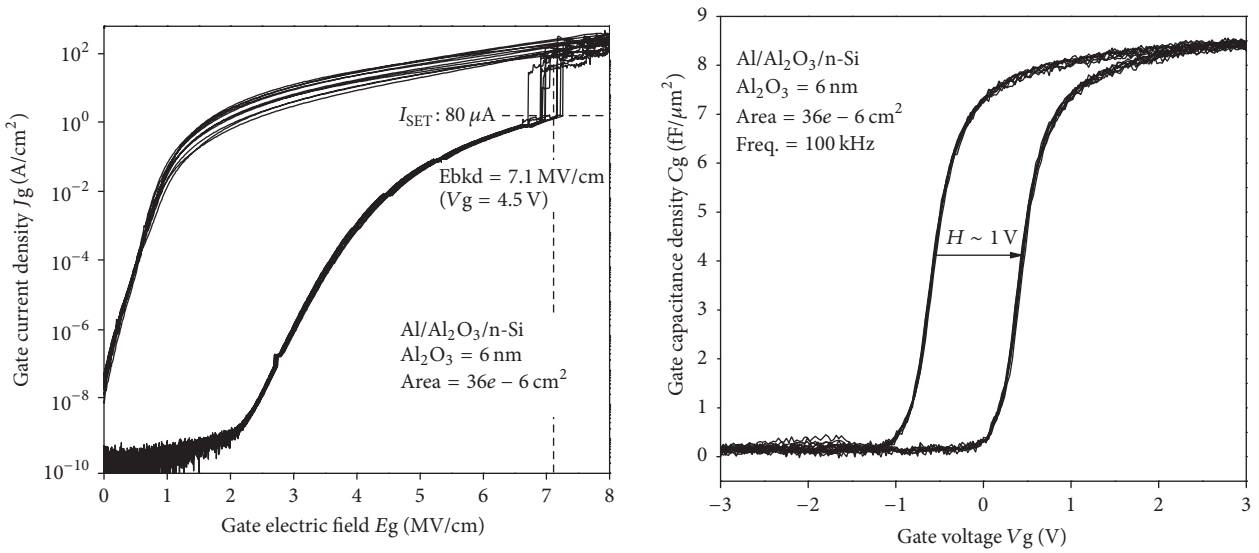


FIGURE 2: Process flow for fabrication of $Al/Al_2O_3/Al$ stacked structures using a maximum temperature of 300°C, ideal for BEOL processing. Traverse cut of an ideal MIM device (where M1 = M2 = aluminum) as well as possible MIM arrays that could be densely integrated within the BEOL stages of an integrated circuit.



(a) *I-V* data MIS devices

(b) *C-V* data MIS devices

FIGURE 3: Electrical characteristics of MIS devices based on thinner Al_2O_3 = 6 nm and without thermal annealing. Outstanding uniformity is observed for both (a) *I-V* and (b) *C-V* data after testing at least 15 different MIS devices for each measurement. This confirms the good quality of ALD method for deposition of thin Al_2O_3.

PF and FN mechanisms were confirmed as the main conduction models with specific trap/barrier energy levels Φ_t/Φ_B for Al_2O_3 [8]. This Φ_t level (PF model) is often associated with some defects and/or impurities in the oxide layer and this makes sense if we consider that some residuals could remain after partial dissolution of the conductive filament. This would impact the reliable operation of a ReRAM device because it will also produce a gradual decrease in the voltage needed for a new SET operation as will be shown later. Also, it is important to notice that a broad resistivity window between the HRS and LRS is obtained for these samples, where 4–6 orders of magnitude secure high endurance during continuous *I-V* resistive cycling of these devices.

For the annealed $Al/Al_2O_3/Al/Glass$ MIM device (with thicker Al_2O_3 = 20 nm), monitoring of the gate current *I*g with time during a constant gate voltage *V*g applied (in the two resistive states HRS and LRS) produces the results shown in Figure 5(a). Initially, large V_{SET} = 3.5 V forces *I*g to

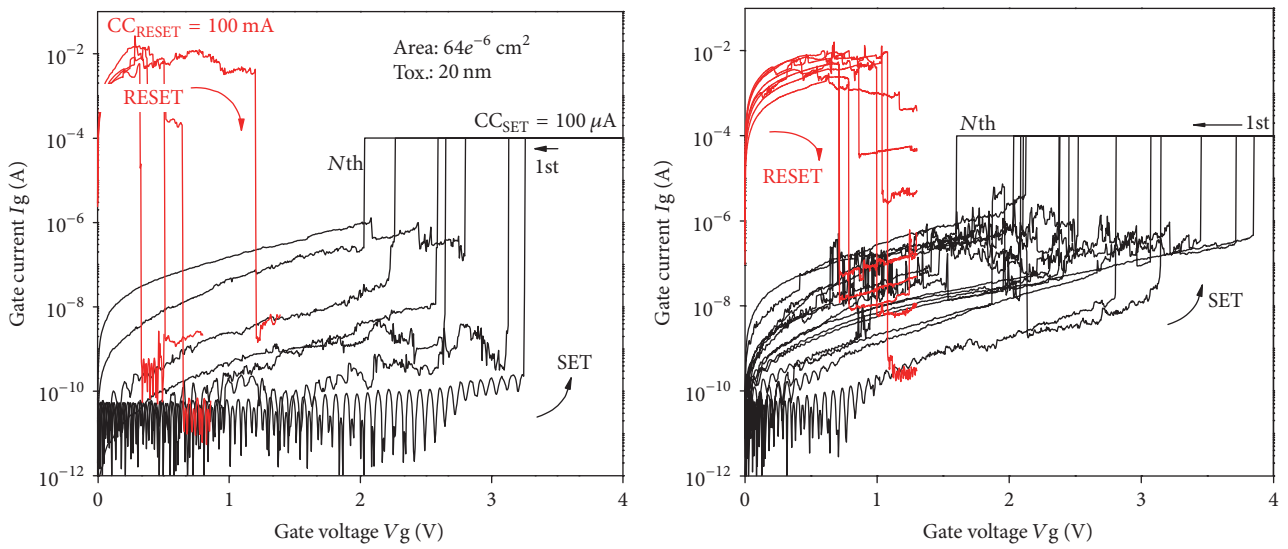


FIGURE 4: Resistive switching of $Al/Al_2O_3/Al$ stacked structures (using thicker Al_2O_3 = 20 nm) for the (a) as-deposited and (b) annealed devices in N_2 at 300°C conditions. The unipolar mode for resistive switching is obtained after using CC_{SET} = 100 μA and CC_{RESET} = 100 mA. A large resistivity window is also observed for both samples.

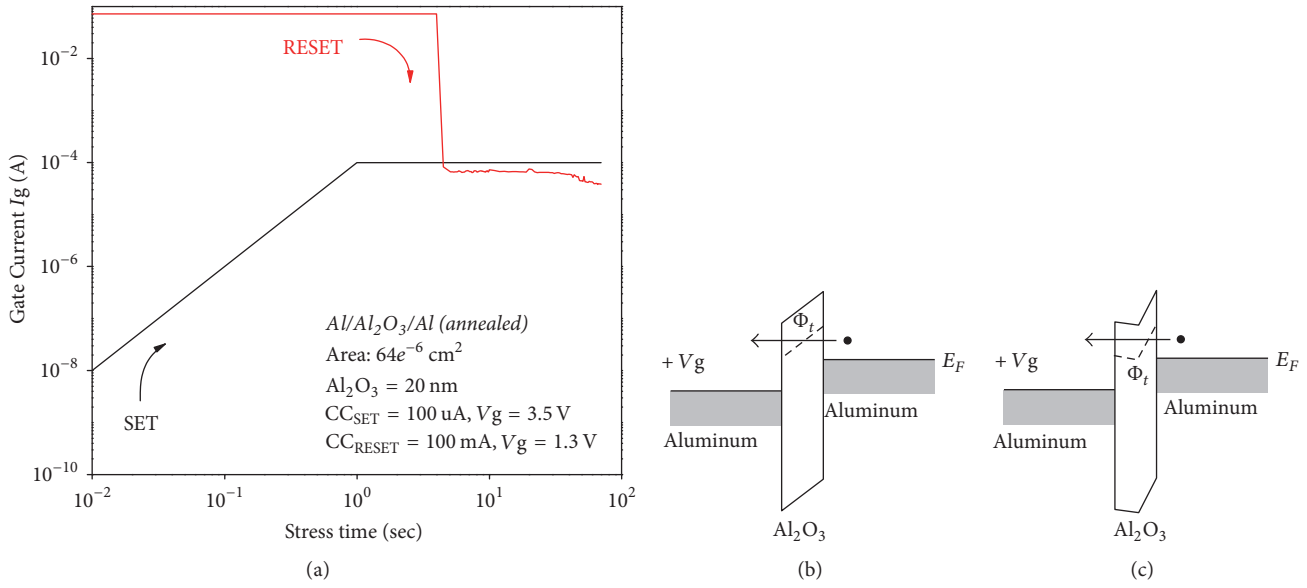


FIGURE 5: (a) Gate current versus stress time for $Al/Al_2O_3/Al$ structure during the SET and RESET conditions. A gradual increase in Ig during the SET condition is evidence of positive charge trapping in the MIM device. Ideal energy band diagrams for the MIM structure under positive bias and where (b) PF tunneling conduction through Φ_t is initiated; (c) a large density of trapped positive charge modifies the energy gap of Al_2O_3.

reach the LRS almost immediately (formation of conductive filament) and it is only limited by CC_{SET} = 100 μA. We notice a gradual increase in Ig with time until CC_{SET} is reached and this is related to continuous trapping of positive charge [9] in the bulk and/or interfaces of Al_2O_3 (enabled by a PF model with a given Φ_t level; see Figure 5(b)). It is thought that a high density of trapped positive charge would be able to modify the energy barriers of Al_2O_3 during tunneling of carriers [9–12] (see Figure 5(c)), so that Ig conduction enhances while progressively reducing V_{SET}. For dissolution of the conductive filament, large CC_{RESET} = 100 mA is required (producing Joule heating) and this produces a sudden decrease in gate current Ig which, in this case, is obtained after the first seconds of stressing bias.

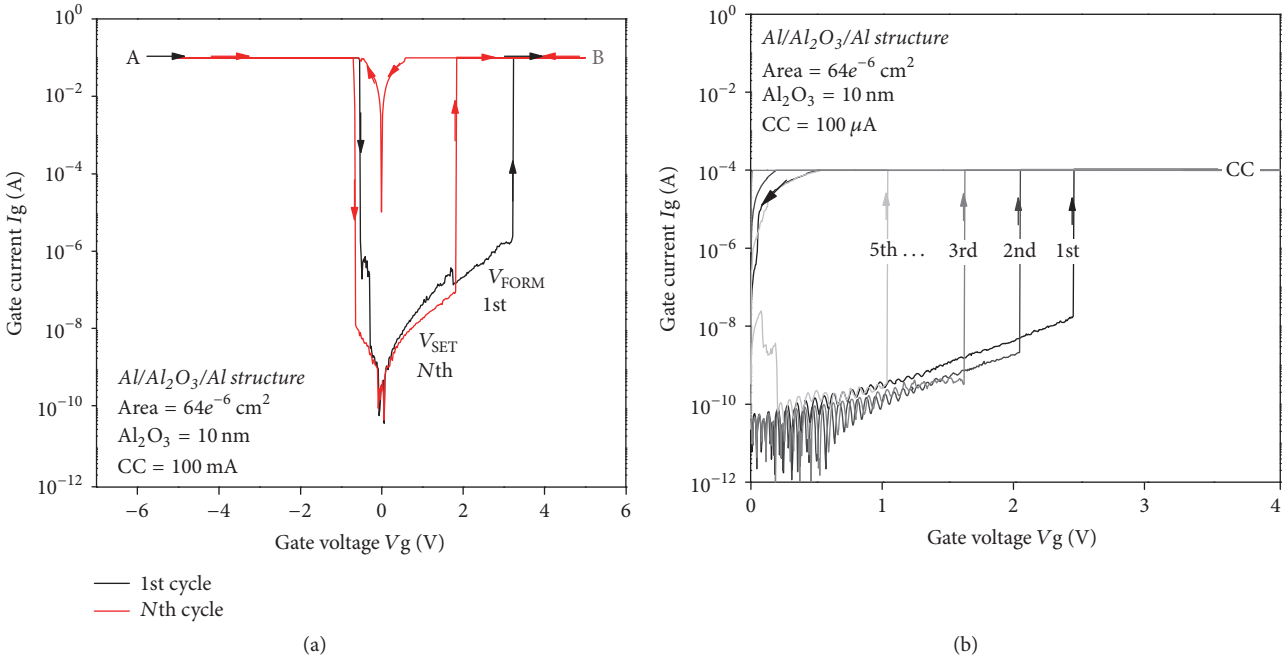


FIGURE 6: Resistive switching for annealed Al/Al_2O_3 (10 nm)/Al stacked structures. (a) Bipolar mode with CC = 100 mA and (b) unipolar mode with CC_{SET} = 100 μA. The I_{OFF}/I_{ON} ratio for these structures is 10^4–10^6 for both operation modes. For the unipolar mode, a decrease in V_{SET} is observed during continuous resistive switching.

Having a large density of trapped positive charge (after the partial dissolution of a conductive filament) will have a profound impact on the endurance characteristics of a ReRAM device. For this, we will examine the electrical characteristics of annealed Al/Al_2O_3/Al/Glass stacked structures having thinner Al_2O_3 = 10 nm. Figure 6(a) shows the first breakdown voltage (forming voltage V_{FORM}) of the memory cell which is larger than the Nth set voltage (V_{SET}) and also the initial current in the HRS is much smaller compared to the current in the LRS as expected. These I-V characteristics correspond to the bipolar switching mode, where a double sweep of voltage (using both polarities) is applied to the same MIM device and I-V hysteretic loops are obtained, while the maximum current is limited to CC = 100 mA. It is important to notice that limiting the maximum current flowing through the device helps to prevent permanent damage of the oxide and therefore more resistive switching cycles could be obtained. For this MIM device, $V_{FORM} > V_{SET}$ and the I_{OFF}/I_{ON} ratio is ~6 orders of magnitude, a large resistivity window able to promote higher endurance during cyclic ReRAM operation. Here, the Nth cycle is the 8th I-V cycle and the gate current at this 8th HRS is lower compared to the 1st HRS, which indicates trapping of negative charge. Whether it was a positive or negative charge, it is clear that a high density of trapped charge is able to decrease V_{SET} in both modes.

For the same MIM structure in the unipolar mode, Figure 6(b) shows that the first transitions to a LRS condition cause a progressive reduction in V_{SET} (during sequential switching from HRS to LRS, up to 5 cycles) in the same device. Here, the corresponding HRS ← LRS transitions are not shown for clarity purposes. Again, even though a large resistivity window is also obtained (4–6 orders of magnitude), a progressive reduction in V_{SET} will compromise both the endurance and other reliability parameters for these memory devices. The exact physical origin for this reduced V_{SET} is out of the scope of this work but there is plenty of evidence pointing to (1) the chemical reduction of Al_2O_3 into off-stoichiometric Al_xO_y after oxygen scavenging by the BE/TE metal layers [13, 14] (thus decreasing the total dielectric constant) and/or (2) metal migration from the BE/TE into Al_2O_3 so that a localized conductive nanofilament (formed by a SET process) could be partially dissolved by a RESET process [6, 7], thus reducing both the effective oxide thickness and the next V_{SET} needed for a new HRS → LRS transition (see Figure 7(a)). Since these memory devices can have two types of switching modes (unipolar and bipolar), each switching mode will mainly depend on the applied bias conditions, on the magnitude of the compliance currents that will limit the total current after breakdown, and, more importantly, on the energy required to transport electronic and/or ionic (oxygen vacancies and metal ions) charge for cyclic formation and rupture of conductive filaments. It is important to notice that, for both the bipolar and unipolar modes, the minimum current compliance during continuous resistive switching of this device is set to CC ≥ 100 μA. It has been recently demonstrated that the level of CC fixed for memory switching is quite important for transitioning between two resistive states of a binary metal oxide [6, 7]. At lower CC < 10 μA, the switching occurs due to a conductive path formed mainly by charged oxygen vacancies [Vo^+], while for CC > 10 μA, the conduction path is formed by metal ions [M^+] that

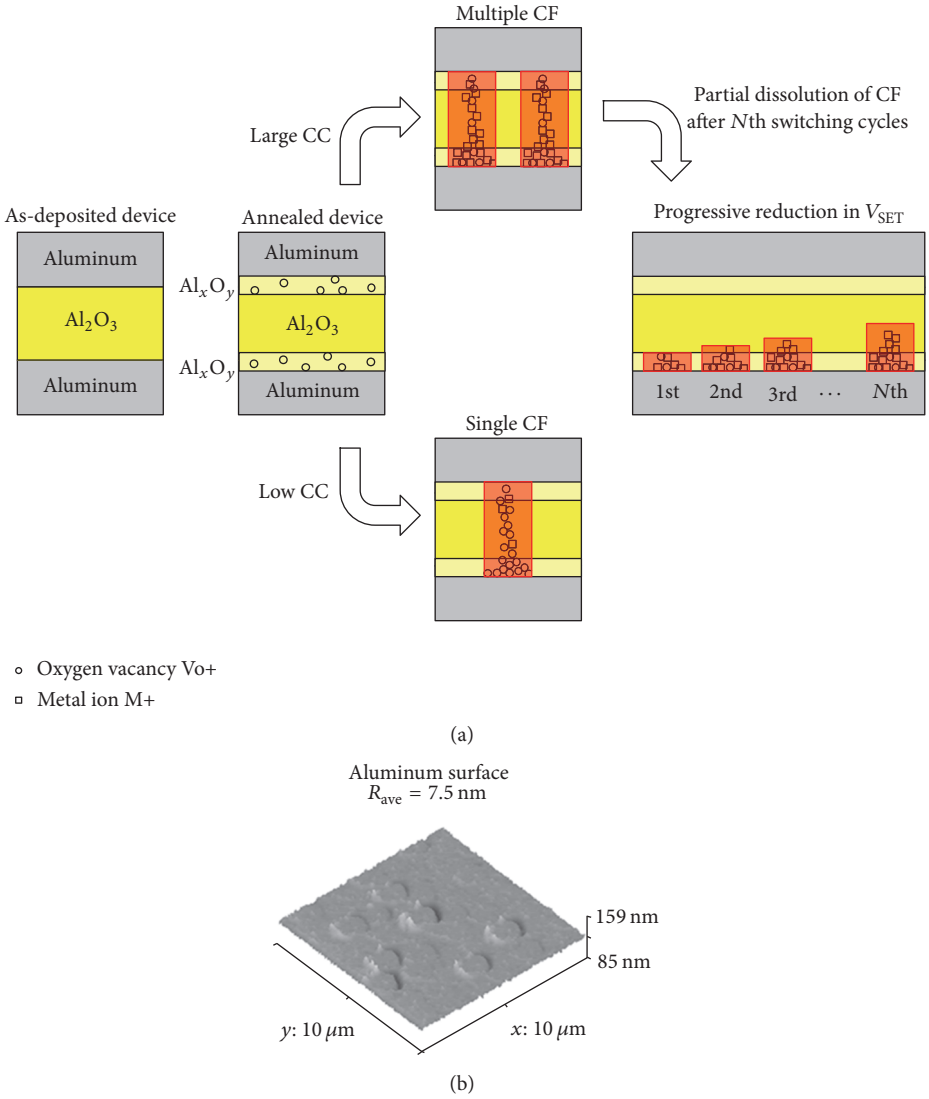


FIGURE 7: (a) Proposed physical mechanism for the origin of single and/or multiple conductive filaments (CFs) for Al/Al_2O_3/Al structure during the SET process (depending on the current compliance limit) and the effect that partial dissolution of this previously formed CF has on the progressive reduction of V_{SET}. For larger CC, multiple formation of CFs should be expected, with their composition being mostly based on metal ions [M^+]. (b) Average surface roughness of the BE (after AFM) showing large surface roughness which is close to the physical Al_2O_3 thickness of the MIM device. High surface roughness would promote local electric-field enhancements.

diffuse or migrate from the metal electrodes (BE/TE) into the oxygen vacancy-rich oxide defect network [15–17]. This is very important, since, depending on the type of species forming the conductive filament (Vo^+ or M^+), any residual left after dissolution of the conductive filament (RESET process) would make the detrapping process from a shallow/deep trap-energy level easier/harder, thus affecting the resistivity windows, endurance, and other reliability issues. Of course, a more precise estimation of the current needed to induce Vo^+ or M^+ based formation of conductive filaments would be normalizing *I*g to smaller device areas or, even better, integrating the injected charge with time [18, 19] because, due to highly different oxide thicknesses, very different current levels would be required. Nevertheless, the oxide thickness regime in our samples is in concordance with the migration thermodynamics for Vo^+/M^+, described quite recently [6, 7]. In our samples, the *I-V* data of Figure 6 already show that CC is set to 100 mA and 100 μA for the bipolar and unipolar switching modes, respectively, thus suggesting that the main species forming the conductive filament (by a SET process) are based on metal ions [M^+] which, in this case, would be some specific oxidation states of aluminum (the same metal material for both the BE and TE). A simplified model showing the physical mechanisms behind a progressive reduction in V_{SET} as well as the surface roughness of the BE is illustrated in Figures 7(a)-7(b). During formation of single/multiple conductive filaments, not only the current compliance but also the surface roughness at the metal/oxide interfaces are important, since this would lead to local electric-field enhancements and then early breakdown [20, 21].

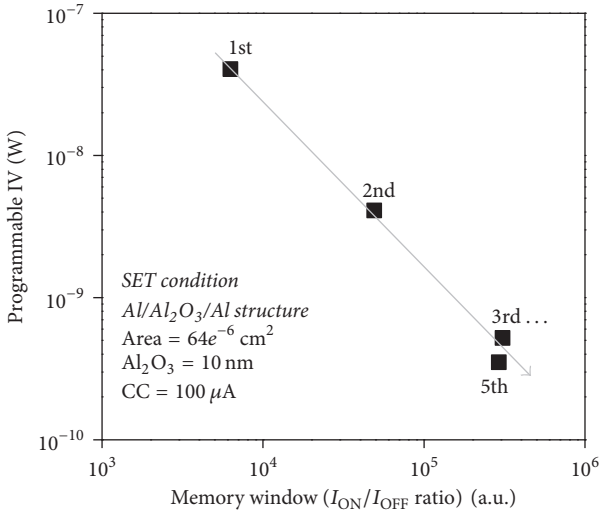


Figure 8: Based on the data of Figure 6(b), the power needed to promote continuous resistive switching of that MIM structure is reduced, while the memory window (I_{ON}/I_{OFF} ratios) increases. Even though these are desirable characteristics for a ReRAM device, this behavior is a consequence of the progressive reduction in the V_{SET} parameter which, in turn, will compromise endurance and the general reliability of these memory devices.

Figure 7(a) suggests that, by using large CC, generation of a single broad conductive filament or generation of more than one conductive filament occurs. Generation of single or multiple conductive filaments is in the end promoted by the total current flowing through the device. We also notice that, by using a sufficiently large CC limit during each switching cycle, a partial dissolution of the CF would mostly leave a high density of metal ions (close to the biased anode) which then results in the progressive reduction of V_{SET} (as observed in Figure 6(b)). Figure 7(b) shows the surface morphology of the first aluminum layer which was used as bottom electrode in the $Al/Al_2O_3/Al$ structure. The average roughness for this aluminum layer is 7.5 nm (which could be related to formation of stacking faults during evaporation of this metal) and since the physical thickness of Al_2O_3 = 10 nm, reducing this severe surface roughness is critical in order to enhance the reproducibility of hysteretic I-V characteristics. Therefore, we could relate the observed variations in V_{FORM}, V_{SET}, and V_{RESET} of Figures 4(a)-4(b) to variations in the physical thickness of the effective oxide, since the roughness [22] at the metal/Al_2O_3 interfaces is almost of the same physical thickness as observed after atomic-force microscopy.

Figure 8 shows the power ($V_{SET} \cdot I_{SET}$) needed to promote the HRS $\rightarrow$ LRS transitions already observed in Figure 6(b) versus the memory window (I_{ON}/I_{OFF} ratios) therein obtained. A seemingly desirable tendency is observed, where, for 5 continuous resistive switching cycles (unipolar mode), less power is required to produce these transitions, while the memory window is also increased. This behavior, however, is due to progressively reduced V_{SET} which, in turn, will severely compromise the endurance and the long-lasting performance of these devices.

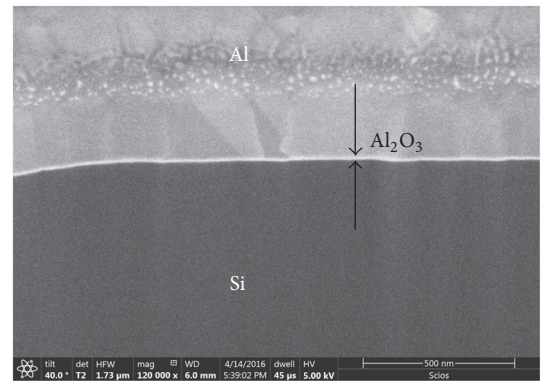


Figure 9: Scanning electron microscopy image for $Al/Al_2O_3/Si$ structure (Al_2O_3 = 20 nm, annealing in N_2 at 300°C) after FIB preparation of a traverse-cut face (using secondary electrons of an intralens detector for morphology imaging). A smooth transition between all materials is observed, while the polycrystalline nature of the metal electrode is also visible.

Figure 9 shows the scanning electron microscopy image (secondary electrons using an in-lens detector) of Al_2O_3-based MIS device (Al_2O_3 = 20 nm, annealing in N_2 at 300°C) in which the ultralow atomic surface roughness of the silicon substrate is used in order to show a relatively smooth transition in the morphology and composition of all the materials used for the stacked structure (seen as a sharp difference in the contrast for all films).

The image shows the "curtaining effect" or ripple formation after focused-ion beam (FIB) preparation [23] of a specific face of this MIS device. Because of the sputtering action of the ion beam, the FIB can be used to locally remove or mill away material (exposing the desired face and its interfaces) while getting surface roughening and shadowing effects due to heavy ion bombardment. Although it is difficult to confirm the chemical reduction of Al_2O_3 into Al_xO_y after annealing (as schematically illustrated in Figure 7(a)), we can observe the high uniformity of the Al_2O_3 film after thermal ALD and even the polycrystalline nature of the aluminum electrode which is the material used for the BE and TE in our MIM devices. This is important given the relatively large gate area for these MIM devices (80 μm × 80 μm), where intrinsic defects directly related to the resistive switching of the high-k layer could be masked by extrinsic defects whenever larger areas are under electrical characterization [24–26].

A full understanding of the complex resistive switching phenomena is still a work in progress to which many research labs across the globe have actively contributed so that, by now, microscopic and nanoscopic details related to migration dynamics of atomic elements within stacked MIM structures have emerged. This is quite important since it could contribute to a better definition of the *"memristor effect"* which by now is still limited to the basic memristor fingerprints [27–29] able to identify a *memristive* device:

(1) The device must exhibit a *"pinched hysteresis loop"* in the voltage-current plane for any bipolar periodic signal excitation. This *"pinched hysteresis loop"* must

converge and cross the origin of this voltage-current plane.

(2) The pinched hysteresis loop area should decrease monotonically as the excitation frequency increases.

(3) The pinched hysteresis loop should shrink to a single-valued function when the frequency tends to infinity, which is similar to turning a memristor into a common resistor, where well-defined linear *I-V* dependence is observed.

Nevertheless, this work tries to identify and correlate some issues that occur simultaneously in MIM devices during cyclic resistive switching measurements: (a) the origin of variations in the resistive switching phenomena of $Al/Al_2O_3/Al$ devices in both the bipolar and unipolar modes, (b) the modeling of a mechanism responsible for these variations (combining physical, chemical, and electronic phenomena) and whose more accurate details, occurring at the nanoscopic level, have been demonstrated for even higher dielectric constant materials like HfO_2 [24–26, 30, 31], and (c) the connection of the former points from the perspective of the formation/dissolution of conductive filaments. All these issues are of the utmost importance in order to provide a more precise physical explanation regarding the operation mechanism of ReRAM devices and, therefore, enabling the development of accurate electrical models (not only for the DC regime but also for frequency-dependent conditions) that could accelerate the research and application of nonlinear phenomena with these memristive materials and devices.

4. Conclusions

MIM based ReRAM devices (using symmetric $Al/Al_2O_3/Al$ structures) have been fabricated at low processing temperatures and the *resistive switching* effect has been observed for both the bipolar and unipolar operation modes which are dependent on the amount of electrons tunneling through the device. For cyclic ReRAM operation, $V_{FORM} > V_{SET} > V_{RESET}$ was found and a relatively large I_{OFF}/I_{ON} ratio of 4–6 orders of magnitude is useful for higher endurance. In the unipolar switching mode and by measuring several resistive switching cycles in the same sample, V_{SET} is progressively reduced and that might be related to a combined mechanism of (a) incomplete dissolution of conductive filaments (made of oxygen vacancies and, mostly, metal ions) which leaves some residuals close to the anode and (b) thickening of chemically reduced Al_2O_3 during localized Joule heating. Also, even though high uniformity of thicker Al_2O_3 films is observed in MIS devices after SEM imaging, the surface roughness of the aluminum-based bottom electrode (after AFM analysis) is close to the physical thickness of Al_2O_3 itself, thus compromising the performance and general reliability of these MIM devices by localized electric-field variations. Nevertheless, these samples have shown the memristor effect while using low-temperature processing and standard materials used in the BEOL stages of an integrated circuit. By optimizing the physical and processing parameters of this structure, vertical integration of dense memory arrays using MIM structures could be implemented at BEOL processing in order to obtain denser, smarter, and more efficient integrated circuits. Given the importance of memristive devices (also memcapacitive and meminductive elements) for modeling nonlinear phenomena, experimental evidence relating resistive switching behavior to microscopic and nanoscopic details of conductive filament formation is necessary in order to use better models for the analysis, design, and simulation of memristor-based circuits (with analog, digital, logic, neuromorphic, secure communications and several other applications).

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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