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September 20, 2005

Power Supply Ripple Rejection and Linear Regulators: What's all the noise about?

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'Peace and quiet' is a scarce commodity in our lives, and with the relentless demand for highly integrated, low cost mixed-signal system-on-chip (SoC) solutions [1], it is even less frequent in integrated circuits (ICs). Densely populated SoC environments are plagued with broad-spectrum noise generated from low and high frequency digital, radio frequency (RF), and switching power supply circuits, reaching hundreds of milli-volts and extending from several thousand to a few giga-Hertz [3]. As power supplies drive these rapidly changing loads, noise is created in the supply busses and therefore propagated throughout the chip. It creates jitter and generally deteriorates the dynamic range and spectral fidelity of sensitive analog functions like data converters, phase-locked loops (PLLs), voltage-controlled oscillators (VCOs), and the like [3-6], which is how and why linear regulators have come to amass so much demand.

Linear regulators, among other things, are tasked with shielding sensitive analog blocks from noise in the supplies, making wide-spectrum power supply ripple rejection (PSRR) a vital specification parameter. In broad terms, the function of the regulator is to generate an *independent* supply voltage through a series-shunt feedback network. Figure 1 illustrates the basic architecture of a low dropout (LDO) linear regulator whose added function is to sustain low input-output voltage differentials, which is critical, for instance, in low voltage, battery-supplied applications. Shunt feedback is accomplished by sensing the output voltage through the R_1-R_2 feedback network, comparing it against a stable voltage reference, and generating a corresponding error-control signal to a pass device via an error amplifier. In essence, the feedback control signal will do whatever it takes to ensure the output voltage is close to the reference, and how close is determined by the loop gain ($A_{ol}\beta$) of the circuit.
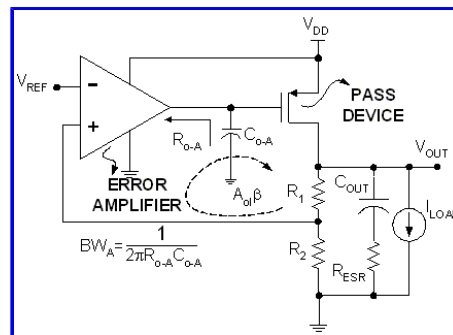

Figure 1. Block diagram of a typical low dropout (LDO) linear regulator

Catching the wave of integration and the demand for point-of-load (POL) regulation, many load-specific LDOs are now being deployed on-chip with output currents in the range of 10 to 50 mA [7-9]. Many of these LDO circuits, unfortunately, do not enjoy the luxury of off-chip capacitors because of the pin- and board-limited nature of the densely integrated systems they serve. Historically, however, designers have relied on these large external passives to shunt away output noise. Today, IC designers are confronted with more noise and less capacitance with which to fight it, with on-chip capacitors ranging only up to 200 pF.

The basic problem…

The problem is the limited bandwidth of the feedback loop; in other words, its ability to regulate the output against fluctuations in the supply is only effective within its bandwidth, which is generally between a few to several thousand Hertz. Shunt capacitors are therefore used to bridge the spectral gap and shunt out higher frequency components of the noise, but on-chip capacitors can only do so at very high frequencies. Traces 1 and 2 in Figure 2 exemplify the typical frequency response of LDOs.
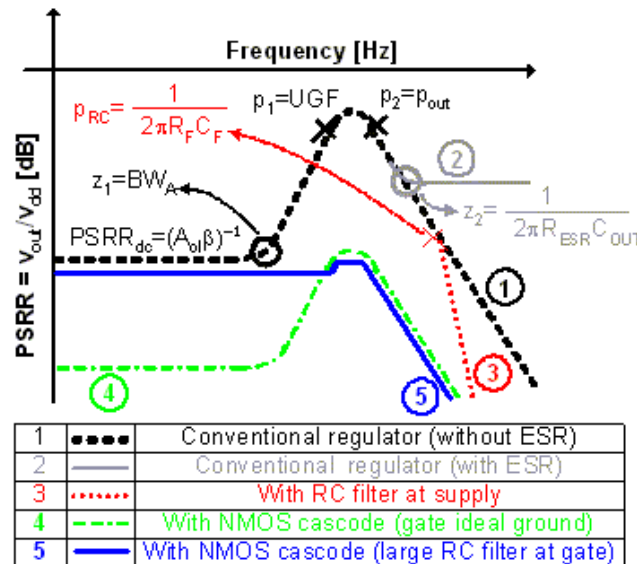

1	▬▬▬▬	Conventional regulator (without ESR)
2	────	Conventional regulator (with ESR)
3	••••••	With RC filter at supply
4	── ── ──	With NMOS cascode (gate ideal ground)
5	────	With NMOS cascode (large RC filter at gate)

Fig. 2. Power supply ripple rejection (PSRR) performance of LDOs

At DC, good PSRR performance is achieved and is inversely proportional to the loop gain. When the loop gain reaches its bandwidth (BWA), gain and therefore PSRR start to deteriorate, as denoted by zero z_1. When the loop gain surpasses its unity-gain frequency (UGF), it no longer plays a factor in the circuit and PSRR is determined by the simple resistive ladder comprised of the pass device, feedback resistors, and load; in other words, PSRR becomes a constant at UGF (p_1) (Traces 1 and 2 flatten at p_1). The output capacitor soon thereafter starts shunting the output signal, at output pole p_{out} (p_2), thereby improving PSRR from that point forward. Eventually, the impedance across the capacitor is much smaller than its equivalent series resistance (ESR) and PSRR is then determined by the resistor-divider network comprised of the pass device and the output capacitor's ESR (ESR is much smaller than the resistor ladder and load resistance), which is when PSRR is again constant and flat (Trace 2 after z_2).

Improving PSRR with only on-chip capacitors

A brute-force method of improving PSRR is to filter the noise before it ever reaches the LDO with another LDO (Figure 3(a)) [4], doubling PSRR but not extending its spectral reach (same limitations exist for the additional LDO as they did for the original). Apart from its spectral deficit, the circuit solution consumes more power and requires more voltage headroom to operate, both of which are detrimental to battery-powered electronics. Similarly, to extend the frequency reach of PSRR, an RC filter can be placed between the supply and the LDO (Figure 3(b)), effectively shunting high frequency noise, as shown by Trace 3 in Fig. 2 with P_{RC}. The series resistor, however, not only increases the dropout voltage of the circuit by $I_{Load}R$ but also consumes significant additional power ($I_{Load}R^2$). Decreasing the value of the resistor while still shunting noise at relatively low frequencies, of course, implies large capacitor values, which are prohibitive for on-chip realizations.
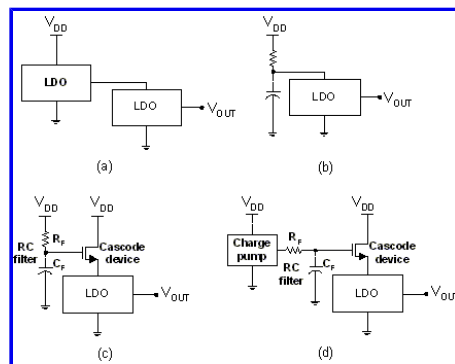

Figure 3. Improving PSRR

So how can supply noise be filtered without a series resistor? The NMOS cascode device shown in Figure 3(c) does just this. It provides a high resistance path to the supply via its saturated drain-source resistance and shunts away supply noise before it is injected to the LDO with a low frequency RC filter. In this case, the source follower's gate is free of high frequency noise and the filter's resistance is not in series with the input supply and therefore does not conduct any DC current. As a result, the resistor can be large without increasing dropout voltage or power losses. Unfortunately, the source follower incurs the dropout voltage degradation that the resistor did not ($V_{dropout} = V_{dropout\_LDO} + V_{GS}$), which is why a charge pump is added in Figure 3(d) ($V_{dropout} = V_{dropout\_LDO} + V_{DS\_sat}$).

The PSRR performance of the charge-pump boosted NMOS cascode circuit is shown in Figure 2 with Trace 5. The filter, since now resistor R_F can be large, is designed to start shunting noise at the loop gain's bandwidth (BW_A), effectively canceling the adverse effects of the bandwidth and never letting PSRR degrade beyond its good low frequency performance. The RC filter also suppresses the systematic ripple generated by the charge pump itself.

An AMI's 0.5µm CMOS charge-pump boosted NMOS cascode LDO was designed and simulated to source 10 mA and regulate 1.0 V (we are now in the midst of preparing a chip prototype). The corner frequency of the RC filter is 3 kHz using a 700 kΩ resistor and 70 pF capacitor combination. The worst-case PSRR under worst-case conditions (low supply voltage and high load current) occurs at 10 MHz and the circuit suppresses this noise by 46 dB, as shown in Figure 4 where a 200 mV, 10 MHz pulse is attenuated to 1 mV.
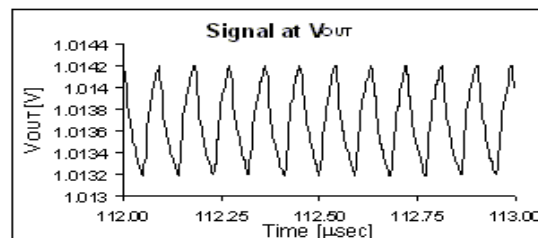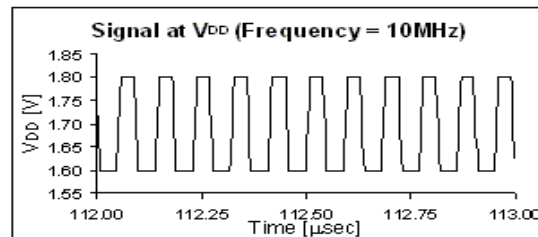
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