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Research Article

Fractional-Order Memristor Emulator Circuits

C. Sánchez-López,[1] **V. H. Carbajal-Gómez**,[1] **M. A. Carrasco-Aguilar**,[1] **and I. Carro-Pérez**[2]

[1]*UATx, Mexico*
[2]*ITESM, Mexico*

Correspondence should be addressed to C. Sánchez-López; carlsanmx@yahoo.com.mx

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This brief leads the synthesis of fractional-order memristor (FOM) emulator circuits. To do so, a novel fractional-order integrator (FOI) topology based on current-feedback operational amplifier and integer-order capacitors is proposed. Then, the FOI is substituting the integer-order integrator inside flux- or charge-controlled memristor emulator circuits previously reported in the literature and in both versions: floating and grounded. This demonstrates that FOM emulator circuits can also be configured at incremental or decremental mode and the main fingerprints of an integer-order memristor are also holding up for FOMs. Theoretical results are validated through HSPICE simulations and the synthesized FOM emulator circuits can easily be reproducible. Moreover, the FOM emulator circuits can be used for improving future applications such as cellular neural networks, modulators, sensors, chaotic systems, relaxation oscillators, nonvolatile memory devices, and programmable analog circuits.

1. Introduction

Resistors, inductors, capacitors, and memristors are basic network elements and the real behavior of each of them is time-varying and nonlinear [1–3]. For the last three cases, the real behavior of each element has always been modeled from integer-order differential equations. However, it is well known that this kind of modeling is only a narrow subset of fractional calculus, which is a generalization of arbitrary order differentiation and integration, and this last approach can be used to better model the description of natural phenomena [4–8]. In this context, fractional calculus is beginning to be used for describing the behavior of memristive elements and systems, i.e., memristors, memcapacitors, meminductors, and any combination of them. Particularly, few studies have been realized on fractional-order memristors (FOM). Thus, [9] analyzes the FOM state equation behavior when a step signal is applied and demonstrates that by controlling fractional parameters associated with the FOM, the saturation time of the resistance can be controlled. In [10], fractional calculus is used to generalize the memristor and higher-order elements, although without any physical meaning. From a mathematical point of view, [11] reports the memfractance concept and according to the fractional-order, it shows the interpolated characteristics between different memristive elements. In [12], the relationship between fracmemristance and fractance is discussed. By combining capacitors together with memristors, net-grid-type structures were also described to approximate the capacitive and inductive fracmemristor. In [13], the no ideal fractional interaction between flux and charge of a memristor is described. However, a piecewise nonlinear model of the memristor is considered and as a consequence, the fractional-order dynamic system is approached but again without any deep physical understanding. More recently, [14] reports the use of Valsa-algorithm for approximating a fractional-order capacitor. Afterwards, this element is substituting the integer-order capacitor into a memristor emulator circuit, obtaining the FOM behavior. However, the main disadvantage of [14] is that not only large RC-circuits are obtained, but the numerical value of each resistive and capacitive element is not commercially available and hence, parallel-series networks must again be used. Despite the FOM concept has been mathematically studied and ideal numerical results were shown, neither physical solid-state device nor emulator circuit has been developed until today. In this scope, this paper addresses

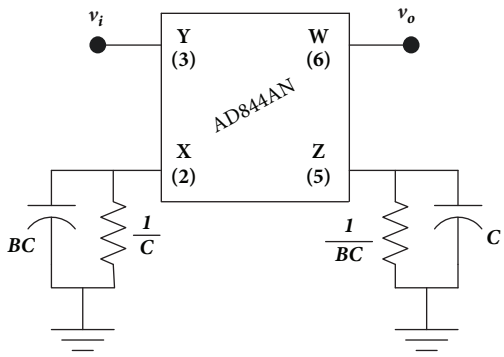


Figure 1: FOI circuit synthesis based on CFOA.

the synthesis of FOM emulator circuits from integer-order memristor emulator circuits previously reported in the literature [15–18]. The rest of the paper is organized as follows. In Section 2, a novel fractional-order integrator (FOI) topology based on current-feedback operational amplifier (CFOA) and integer-order capacitors is discussed. In Section 3, the FOI previously designed is replacing the integer-order integrator (IOI) inside flux- or charge-controlled memristor emulator circuits, at their floating and grounded versions, and the FOMs can also be configured for operating at incremental or decremental mode [2]. Section 4 shows HSPICE simulation results, showing that the fingerprints of an integer-order memristor are holding up for their fractional versions. Finally, some conclusions are summarized in Section 5.

2. Fractional-Order Integrator

A challenge at fractional calculus is the building or in best of cases, the approximation of fractances [19, 20]. In this sense, several mathematical approximations were researched and by its quickly convergence, continuous fractional expansion approach is the most adequate. Thus, the first-order approximation of an FOI is given by

$$\frac{1}{s^{\alpha}} \approx \frac{(1-\alpha)\,s + (1+\alpha)}{(1+\alpha)\,s + (1-\alpha)} = \frac{Bs+1}{B+s}, \qquad B = \frac{1-\alpha}{1+\alpha}\ \forall 0 < \alpha < 1, \tag{1}$$

where α is the fractional-order. It is important to mention that high-order fractance approximations can also be obtained; however, the synthesis of them leads to complex and bulky circuits [21, 22]. A simple circuit able to synthesize (1) is given in Figure 1, whose transfer function is

$$\frac{v_o(s)}{v_i(s)} = A_{v1}A_{v2}A_i\frac{Bs+1}{B+s} \approx \frac{1}{s^{\alpha}}, \tag{2}$$

where $A_{v1,2} \approx 0.98$ and $A_i \approx 0.98$ are the voltage and current gains of the voltage and current followers associated with *X*-*Y*, *W*-*Z*, and *Z*-*X* terminals of the CFOA, respectively. To design the FOI, we propose the following design guide:

(1) Given α, use (1) to compute B.

(2) Choose $C = 0.1\,\text{mF}$ and evaluate $R = C^{-1} = 10\,\text{k}\Omega$.

(3) Using the numerical value of B obtained in the first step, evaluate BC and $R_f = (BC)^{-1}$ of Figure 1. Resistances with noncommercial values are adjusted with precision potentiometers and capacitances with series and parallel connections.

(4) Frequency denormalization is done for $C^{\text{new}} = C/kf$, where kf is the denormalization constant.

Following these steps and from (1), we assume $\alpha = 0.99$, 0.75, 0.50, 0.25, 1 m, and as a consequence $B = 5$ m, 0.14, 0.33, 0.60, 0.99; $V_{dd} = \pm 10$ V, $v_i(t) = A_m \sin(\omega t)$, where $A_m = 2$ V is the amplitude of the voltage signal source, $\omega = 2\pi f$, $f = 20$ kHz, and $kf = 50$ k. According to the third and fourth steps, BC/kf = 10 pF, 0.28 nF, 0.66 nF, 1.2 nF, 2 nF, $R_f = (BC)^{-1} = 2\,\text{M}\Omega$, 70 kΩ, 30 kΩ, 16.6 kΩ, 10 kΩ, and $C/f = 2$ nF. To make a fair comparison, an IOI is obtained of Figure 1 by removing $(BC)^{-1}$ and BC. In this way, Figures 2(a)–2(e) illustrate the transient behavior of the FOI for each α described above and one can observe that for $\alpha = 0.99$ (Figure 2(a)), the behavior of the FOI approximates to IOI, whereas for α = 1 m, $B \approx 1$ and hence, Figure 1 becomes a voltage follower, as described in (2) and depicted in Figure 2(e) [23]. Note that, for all graphics, HSPICE results are in agreement with experimental results. Moreover, from point of view of root locus analysis, the zero and pole of (2) are moved when α varies. This is a serious disadvantage, since C should quickly be discharged when R_f is low. To mitigate this problem, the pole is set up and fixed for $\alpha = 0.99$ and the FOI behavior is plotted when the zero is varied. Figures 2(a)–2(e) show that this assumption can still model the behavior of FOI with a low error level. Nevertheless, when $\alpha = 1$ m, the error increases and the pole is not placed on the zero. Hence, Figure 1 becomes again a voltage follower, but with a light phase shifting, as depicted in Figure 2(e). For convenience, the magnitude and phase response in the frequency domain of Figure 1 for the three cases (IOI, FOI, and FOI with R_f fixed) and when α varies are illustrated in Figure 3. In the former figure, one can observe that the magnitude response has slope -20α dB/dec which decreases when α also decreases. Notice that when $\alpha = 0.99$, the magnitude response of the three cases is superimposed and with 49.42 dB at DC. Afterwards, when α is monotonically decreased, the magnitude and slope of the second and third case are modified. Thus, for $\alpha = 0.75$, the magnitude at DC of the second case is 16.45 dB and from 3 kHz, this is superimposed with the magnitude of the first case. Later, when α takes the aforementioned values and from 20 kHz, the frequency responses of the second and third cases are similar, as shown in Figure 3(a), confirming the previous analysis [20]. Note that, at low-frequency, the magnitude of the FOI varies for the different values of α, whereas the magnitude at DC of the third case remains at 49.42 dB. Moreover, Figure 3(b) shows the phase response given by $\theta = -90^{\circ}\alpha$ or $\theta = -\pi\alpha/2$ rad. Similarly as above, when $\alpha = 0.99$ the phase response for all cases is superimposed at -90°. This behavior is modified for second and third cases, and when α takes different values. Therefore, for FOI, one can observe in Figure 3(b) that the phase becomes zero when $\alpha = 1$ m,

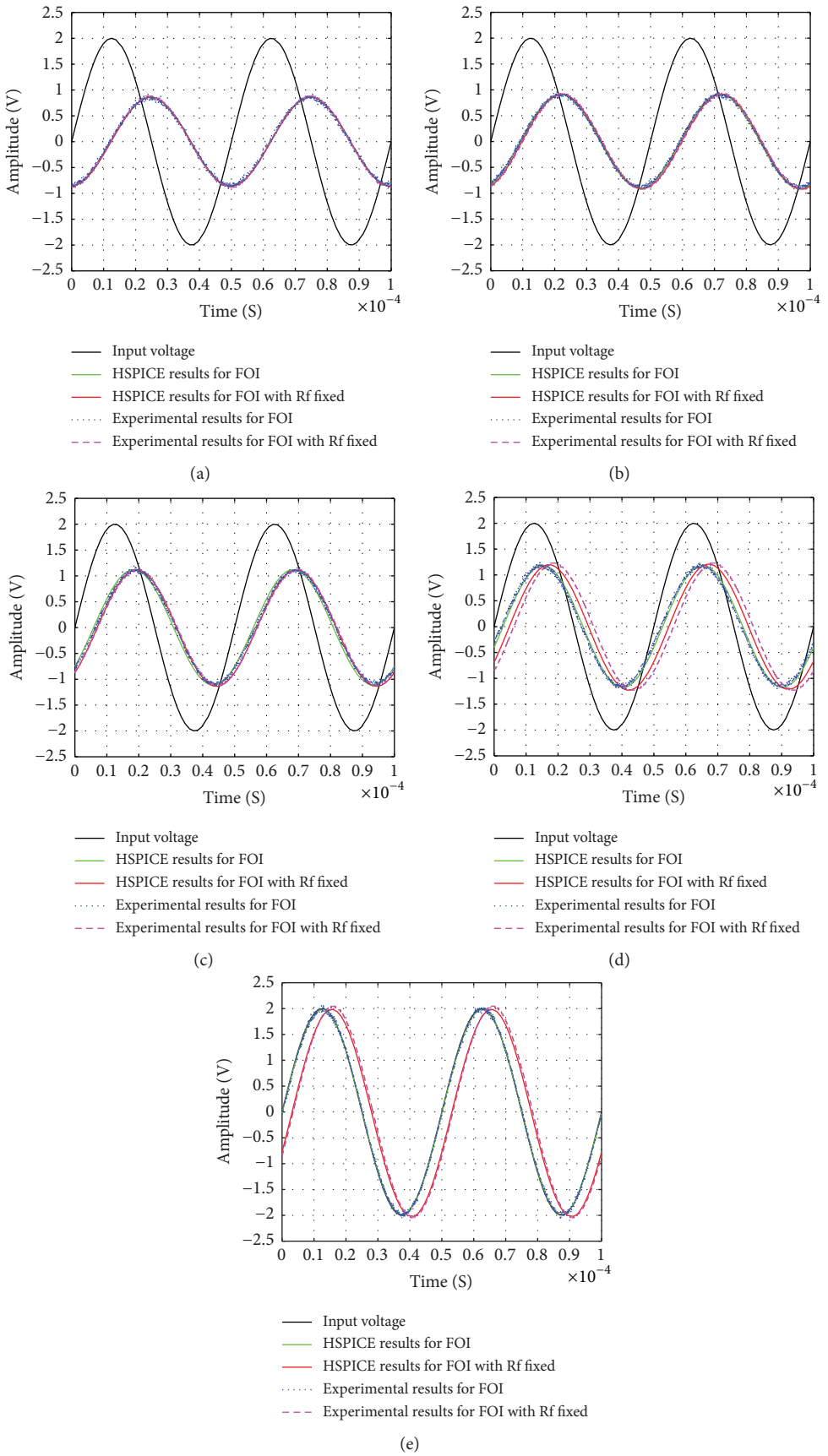
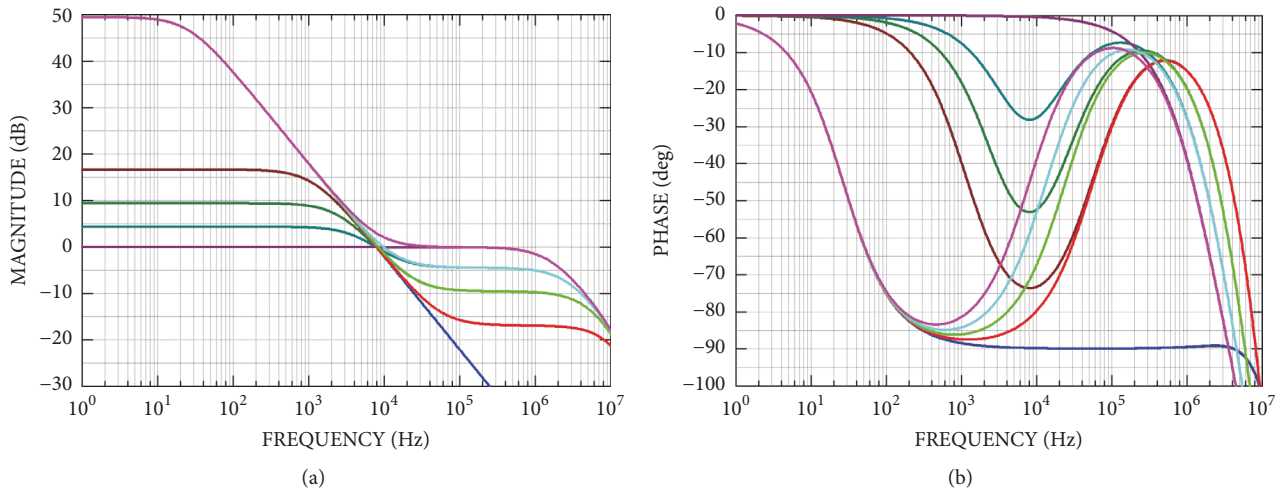


FIGURE 2: Transient responses of IOI, FOI, and FOI with R_f fixed when (a) $\alpha = 0.99$, (b) $\alpha = 0.75$, (c) $\alpha = 0.5$, (d) $\alpha = 0.25$, and (e) $\alpha = 1$ m, all operating to $f = 20$ kHz.



(a) (b)

Figure 3: Behavior of IOI (black line), FOI for: $\alpha = 0.99$ (blue line), $\alpha = 0.75$ (red line), $\alpha = 0.5$ (green line), $\alpha = 0.25$ (cyan line), and $\alpha = 1\,\text{m}$ (magenta line); and FOI with R_f fixed for $\alpha = 0.99$ (light blue line), $\alpha = 0.75$ (light red line), $\alpha = 0.5$ (light green line), $\alpha = 0.25$ (light cyan line), and $\alpha = 1\,\text{m}$ (light magenta line): (a) magnitude response and (b) phase response.

Table 1: Numerical values of the phase and magnitude response of IOI, FOI, and FOI with R_f fixed for $\alpha \in (0, 1)$ and $f = 20\,\text{kHz}$.

α	Phase (Deg)				Magnitude (dB)			
	IOI	FOI	FOI with R_f fixed	Difference	IOI	FOI	FOI with R_f fixed	Difference
0.99	−89.92	−89.91	−89.91	0	−8.25	−8.25	−8.25	0
0.75	-	−66.71	−69.89	3.18	-	−7.71	−7.70	−0.01
0.5	-	−42.27	−49.66	7.19	-	−5.93	−5.85	−0.08
0.25	-	−20.31	−33.44	13.13	-	−3.19	−2.96	−0.23
1 m	-	−0.88	−22.09	21.21	-	0.072	0.541	0.469

whereas a level of error is glimpsed for FOI with R_f fixed. From these graphics, we can claim that the proposed topology is stable until 1 MHz, approximately [24]. Table 1 gives the numerical value of the magnitude and phase response for $f = 20\,\text{kHz}$ and different α. It is important to mention that, for any design where $\alpha > 1$ is required, the FOI must be connected in cascade with q integer-order integrators, such that $\widehat{\alpha} = \alpha - q$. For instance, let us suppose $\alpha = 4.35$; then $q = 4$ and $\widehat{\alpha} = 4.35 - 4 = 0.35$.

3. Fractional-Order Memristor Synthesis

In [15], a flux-controlled floating memristor emulator circuit which uses four positive second-generation current conveyors (CCII+s) and one analog multiplier was reported. According to Figure 1 in [15], the topology has an IOI circuit well defined and its memristance equation given by (9) in [15] is also of integer-order. To obtain an FOM from integer-order memristor, the integrator circuit of the latter must be replaced by FOI circuit, as shown in Figure 4(a). Following the analysis given in [15, 25], the behavioral model is deduced as

$$\frac{v_m(t)}{i_m(t)} = R_1 \pm \frac{R_4}{10R_2}\left(R_1 - \frac{V_V}{i_m(t)}\right) {}_aJ_t^{\alpha} v_m(t) - \frac{V_H}{i_m(t)}, \quad (3)$$

where V_H and V_V are DC voltage sources to control horizontally and vertically the offset of the dependent-frequency pinched hysteresis loop on the voltage-current plane, respectively [25], and ${}_aJ_t^{\alpha}$ denotes the fractional-order integral operator of

(i) Riemann-Liouville and Caputo fractional integral

$${}_aJ_t^{\alpha} v_m(t) = \frac{1}{\Gamma(\alpha)} \int_a^t \frac{v_m(\tau)}{(t-\tau)^{1-\alpha}} d\tau, \quad (4)$$

(ii) or Grunwald-Letnikov fractional integral

$${}_aJ_t^{\alpha} v_m(t) = \lim_{h \to 0} h^{\alpha} \sum_{p=0}^{(t-a)/h} \frac{\Gamma(\alpha + p)}{p!\Gamma(\alpha)} v_m(t - ph), \quad (5)$$

where for both fractional integrals, a and t are the lower and upper limits of integration.

Defining the fractional-order flux $\phi_m^{\alpha}(t) = {}_aJ_t^{\alpha} v_m(t)$, (3) can be rewritten as

$$\begin{aligned} \frac{v_m(t)}{i_m(t)} &= R_1 \pm \frac{R_4}{10R_2}\left(R_1 - \frac{V_V}{i_m(t)}\right) \phi_m^{\alpha}(t) - \frac{V_H}{i_m(t)} \\ &= M\left(\phi_m^{\alpha}(t)\right), \end{aligned} \quad (6)$$

where $M(\phi_m^{\alpha}(t))$ is the flux-controlled fracmemristance and can be controlled by applying a voltage or current signal

Table 2: Component list of Figure 4(a), Figure 1 in [15], Figure 4(b), and Figure 5 in [18], assuming $C = 0.1$ mF, $kf = 50$ e3, $\alpha \approx 1$, and $f = 20$ kHz.

Element	Figure 4(a)		Figure 1 in [15]		Figure 4(b)		Figure 5 in [18]		Tolerance
	Inc.	Dec.	Inc.	Dec.	Inc.	Dec.	Inc.	Dec.	
V_H	−37 mV	−75 mV	−40 mV	−70 mV	−49 mV		−50 mV		
V_V	36 mV	76 mV	39 mV	85 mV	−50 mV		−93 mV	−95 mV	
A_m	2 V								
$\pm V_{dd}$	±10 V								
R_1	10 kΩ				9 kΩ				±5%
R_2	1 kΩ		10 kΩ		11.5 kΩ				
R_3	-		2.4 kΩ		-		9.5 kΩ		
R_4	10 kΩ				-		-		
C^{-1}	10 kΩ		-		10 kΩ		-		
$(BC)^{-1}$	2 MΩ		-		2 MΩ		-		
BC/kf	10 pF		-		10 pF		-		±20%
C/kf	2 nF		-		2 nF		-		
$C_z = C/kf$	-		2 nF		-		2 nF		

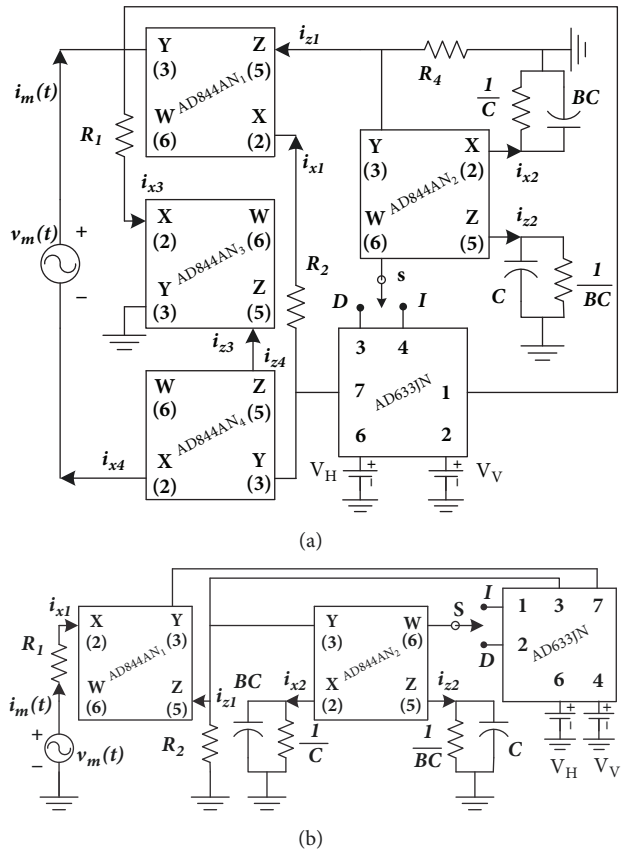


Figure 4: (a) Flux-controlled floating fracmemristor and (b) charge-controlled grounded fracmemristor.

across the memristor, as depicted in Figure 4(a). Moreover, charge-controlled memristor emulator circuits have also been reported in the literature. According to Figure 5 in [18], the emulator circuit has also an IOI circuit and if it is exchanged with Figure 1, then a fractional-order charge-controlled grounded memristor emulator circuit is obtained, as shown in Figure 4(b). Hence, following the analysis given in [18, 25], one obtains

$$\frac{v_m(t)}{i_m(t)} = R_1 \pm \frac{R_2}{10}\left(R_2 + \frac{V_V}{i_m(t)}\right) {}_aJ_t^{\alpha} i_m(t) + \frac{V_H}{i_m(t)} \tag{7}$$

and the fractional-order charge becomes $q_m^{\alpha}(t) = {}_aJ_t^{\alpha} i_m(t)$. Hence, (7) can be written as

$$\begin{aligned}\frac{v_m(t)}{i_m(t)} &= R_1 \pm \frac{R_2}{10}\left(R_2 + \frac{V_V}{i_m(t)}\right) q_m^{\alpha}(t) + \frac{V_H}{i_m(t)} \\ &= M\left(q_m^{\alpha}(t)\right),\end{aligned} \tag{8}$$

where $M(q_m^{\alpha}(t))$ is the charge-controlled fracmemristance. Regarding Figure 4, the **S** switch is used for selecting the kind of fracmemristor, where **I** denotes the incremental topology and **D** denotes the decremental topology. Note that if $V_H = V_V = 0$ and $\alpha = 1$, then (6) and (8) are reduced to their original versions given in [15, 18].

4. Numerical Simulations

Once the behavioral model for each floating and grounded fracmemristor at its incremental and decremental version has been deduced, numerical simulations can be realized. Henceforth, numerical results of the incremental topologies will be shown below in the left-side and for the decremental topologies will be shown in the right-side. On the one hand, to design the integer-order floating memristor working at incremental and decremental mode, the design guideline reported in [15] was used. Table 2 gives the numerical value of each element of Figure 4(a) and Figure 1 reported in [15], with $v_m(t) = A_m \sin(\omega t)$. On the other hand, since it is not possible to deduce, by now, an analytical model to make a frequency analysis [15], each design variable of the fracmemristor was varied in order to adjust the frequency-dependent pinched

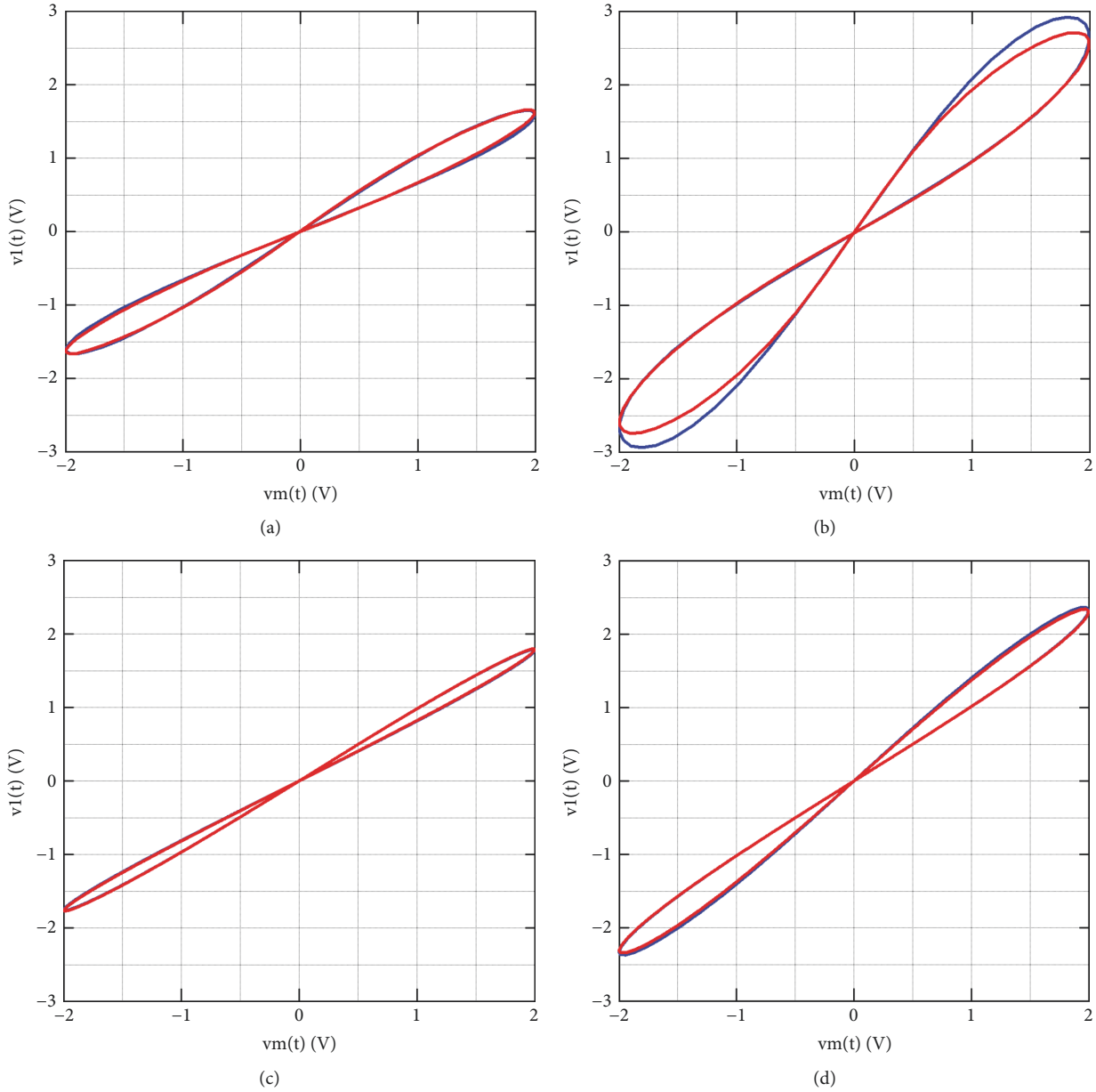


Figure 5: Comparing the frequency-dependent pinched hysteresis loops of the flux-controlled floating memristor (blue line) and fracmemristor (red line): (a) incremental mode, (b) decremental mode, and for the charge-controlled grounded memristor (blue line) and fracmemristor (red line): (c) incremental mode and (d) decremental mode.

hysteresis loop behavior with its integer version. In this way, Figures 5(a) and 5(b) show the pinched hysteresis loops of the flux-controlled floating memristor and fracmemristor at each operation mode and one can observe a good agreement among the graphics for the incremental case. However, a slight variation is glimpsed for the decremental case and could be due to the nonlinearities of the analog multiplier. A similar analysis is done for Figure 4(b) at its integer-order version and Figure 5 taken from [18]. Table 2 also gives the numerical value of each element used in numerical simulations. Thus, Figures 5(c) and 5(d) depict the behavior of each pinched hysteresis loop at each operation mode. For Figure 5(c), one can observe that both hysteresis loops are almost the same and hence, Figure 4(b) becomes an integer-order memristor [18]. Moreover, when the **S**-switch is connected to **D**-terminal and **I**-terminal is grounded, Figure 4(b) is now configured at decremental mode and Figure 5(d) illustrates the hysteresis loops. On this last figure, one can observe a good agreement among them. Therefore, the behavior of Figure 4(b) becomes also an integer-order memristor. Comparing all graphics of Figure 5, we note that, for each case, the area of each lobe of the latter figures is less than the area of each lobe of the former. Nonetheless, the hysteresis loops of Figures 5(c) and 5(d) can be widened by adjusting the numerical value of R_1 or R_2. However, this will have a negative impact, since the hysteresis loops should

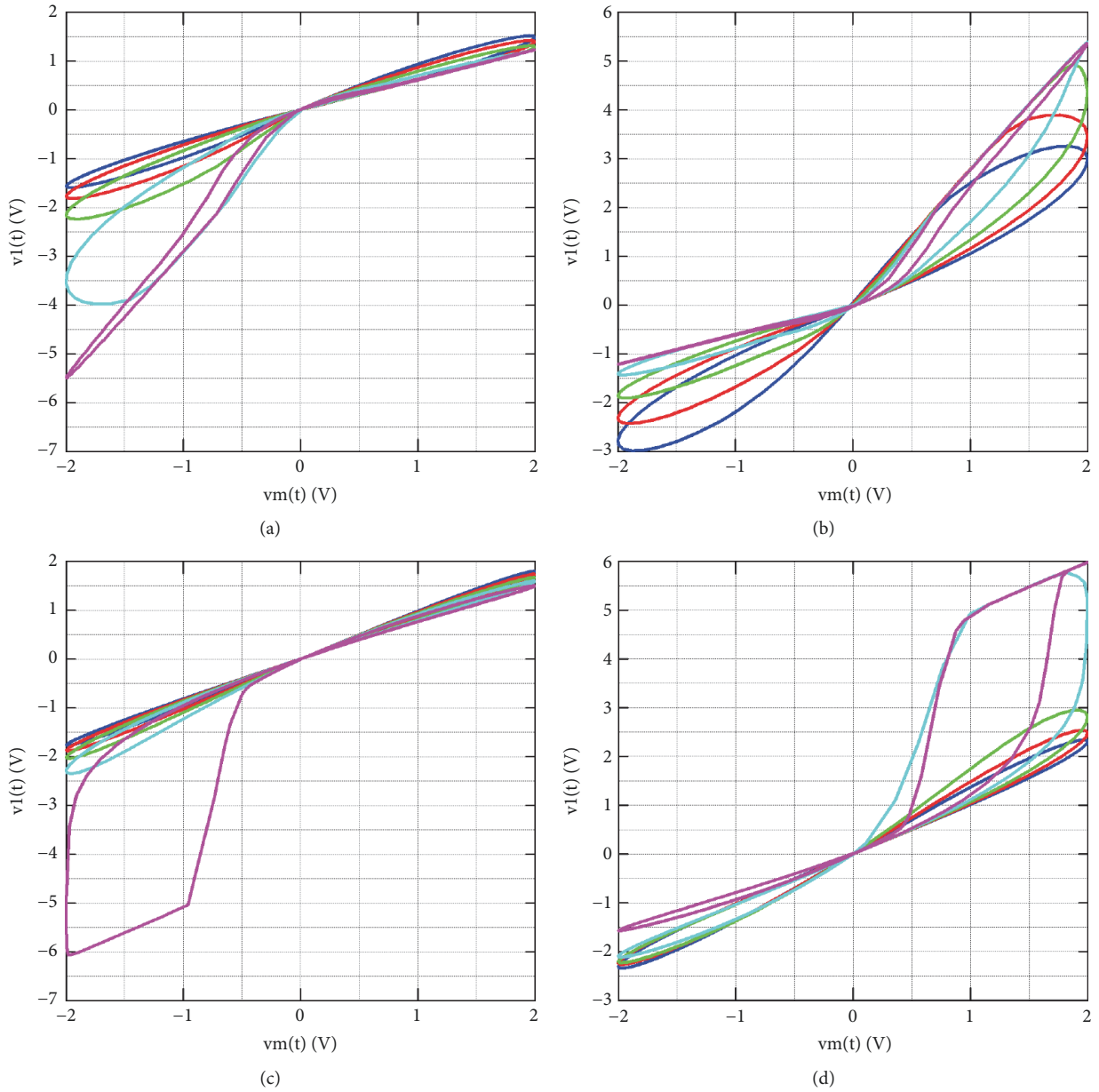


Figure 6: Fractional-order frequency-dependent pinched hysteresis loops of the floating fracmemristor operating at (a) incremental mode and (b) decremental mode. For the grounded fracmemristor operating at (c) incremental mode and (d) decremental mode. For all cases: α = 0.99 (light blue line), α = 0.75 (light red line), α = 0.5 (light green line), α = 0.25 (light cyan line), and α = 1 m (light magenta line).

be lost with a small variation of α. It is worth noting that, unlike [15, 18], the behavior of each frequency-dependent pinched hysteresis loop and at each operation mode has been improved, achieving that, after the offset compensation, all they are operating to 20 kHz and the lobe area of each hysteresis loop becomes relatively equal, obtaining frequency-dependent pinched hysteresis loops almost symmetrical. Furthermore, the real behavior of Figures 4(a) and 4(b) in their integer-order versions was experimentally verified in [15, 18] and Figure 5 shows similar behaviors.

Once obtained the hysteresis loops of the floating and grounded fracmemristor in both operation modes and for α = 0.99, we can now reduce α in order to obtain the behavior of each fractional-order frequency-dependent pinched hysteresis loop. Figure 6(a) shows the hysteresis loops of Figure 4(a) at incremental mode and for five numerical values of α, whereas Figure 6(b) illustrates the fractional hysteresis loops of Figure 4(a) at decremental mode. In both figures, note that, when α = 1 m, the hysteresis loops are seriously deformed and as a consequence, the emulator circuits do not work. This behavior is due to that the FOI becomes a voltage follower, as shown in Figure 2(e) (light green line). Moreover, Figures 6(c) and 6(d) show the fractional hysteresis loops of Figure 4(b) configured at incremental and decremental mode, respectively. On these last figures, we note that when α takes different values, the

Table 3: Component list of Figure 1 when α varies, assuming $C = 0.1$ mF and $kf = 50$ e3.

Element	$\alpha = 0.99$	$\alpha = 0.75$	$\alpha = 0.5$	$\alpha = 0.25$	$\alpha = 1$ m
C^{-1}			10 kΩ		
$R_f = (BC)^{-1}$			2 MΩ		
BC/kf	10 pF	0.28 nF	0.66 nF	1.2 nF	2 nF
C/kf			2 nF		

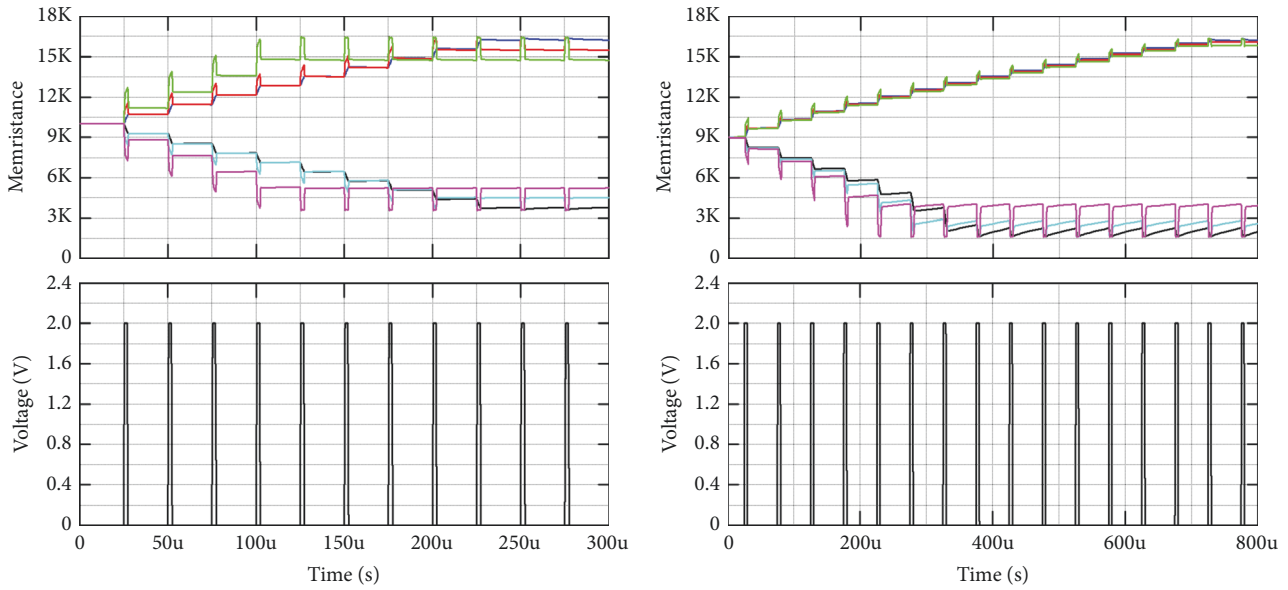


Figure 7: Incremental and decremental fracmemristance variation when a pulse train (bottom graphics) is applied to (a) Figure 4(a) and (b) Figure 4(b). For the incremental case: $\alpha = 0.99$ (light blue line), $\alpha = 0.75$ (light red line), and $\alpha = 0.5$ (light green line). For the decremental case: $\alpha = 0.99$ (black line), $\alpha = 0.75$ (light cyan line), and $\alpha = 0.5$ (light magenta line).

range of variation of the hysteresis loops is shorter than Figures 6(a) and 6(b). Similarly as above, when $\alpha = 1$ m, the emulator circuit does not work. For all graphics of Figures 5 and 6, $v_1(t) = i_m(t)R_1$ was used to indirectly plot $i_m(t)$. At this point, our results indicate that, by selecting adequately the numerical value of each element of Figures 4(a) and 4(b) for a particular operating frequency, both emulator circuits are able to generate fractional hysteresis loops. Table 3 gives the numerical value of each element of Figure 1 for different values of α. However, comparing the linear time-varying parts of (6) and (8) we note that the former has four design variables and the latter only two, limiting the performance range of the emulator circuit when α varies and as a consequence, Figure 4(a) has better performance, as shown in Figure 6. It is worth stressing that our results are confirming the theory given in [10]. Besides the fractional pinched hysteresis loops, other fingerprint of the fracmemristor is when the pinched hysteresis loop shrinks when increasing the excitation frequency and although herein is not shown, each fracmemristor behaves as a time-invariant resistor. Moreover, it is interesting to research other fingerprints related to the fracmemristance, which is the nonvolatility of its fracmemristance. This means that once the fracmemristance is programmed, its last value must be *freezed* during a long time and when the input signal is not applied. Therefore, for Figure 4(a) configured at incremental and decremental mode, a pulse train with 2 V of amplitude, 1.36 μs of pulse width, and 25 μs of period is applied and as illustrated in Figure 7(a) (top graphics), one obtains the incremental fracmemristance change for $\alpha = 0.99$ (light blue line), $\alpha = 0.75$ (light red line), and $\alpha = 0.5$ (light green line), whereas the decremental fracmemristance changes for the same values of α are also obtained and given by black line, light cyan line, and light magenta line, respectively. A similar analysis is done for Figure 4(b) also configured at incremental and decremental mode but with a pulse train of 2 V of amplitude, 4 μs of pulse width, and 50 μs of period. In this way, Figure 7(b) (top graphics) shows the incremental and decremental fracmemristance change for the same values of α and labeled with the same kind of lines described before. Note that, for all graphics, during nonpulse period the fracmemristance is nonvolatile and its variation is negligible. However, an overshoot signal is glimpsed for all fracmemristances and it is due to the behavior of the FOI. Nonetheless, after of the overshoot, each fracmemristance for each α is held up. Furthermore, when α is near to 1, not only the fracmemristances are similar to the memristances and hence, the maximum (17 kΩ for Figure 7(a) and 16 kΩ for Figure 7(b)) and minimum (4 kΩ for Figure 7(a) and 1.64 kΩ for Figure 7(b)) fracmemristance are obtained, but the range

of variation of the former should monotonically be reduced when α decreases and as a consequence, the maximum and minimum fracmemristance are also reduced, as shown in Figure 7. It is worth stressing that the proposed synthesis methodology is only applicable for those integer-order memristor topologies where the IOI circuit is clearly defined, and when it is replaced by FOI circuit, the resulting emulator circuit behavior, in general, is lightly modified.

5. Conclusions

A synthesis methodology for obtaining the behavior of FOM emulator circuits from integer-order memristor emulator circuits at their versions floating and grounded and operating at incremental and decremental mode has been described. Basically, the methodology consists of exchanging the IOI circuit clearly defined in the integer-order memristor emulator circuit by an FOI circuit, so that not only an FOM is obtained, but also the synthesized topology is not drastically modified with respect to its original topology. In each fractional topology, a mechanism of offset compensation in order to push or pull the crossing point of the hysteresis loops towards the origin was used [25] and as a consequence, both fracmemristors are able to operate at high-frequency. However, it is important to mention that, at high-frequency, not only parasitic elements associated with the active devices affect the performance of the emulators, but also the parasitic elements associated with the breadboard or printed circuit board. Therefore, there is a limit on the operating frequency of the emulators, as has already been reported in [16, 17, 26]. It has numerically been demonstrated that the fractional-order frequency-dependent pinched hysteresis loops are reduced when α decreases, but each hysteresis loop becomes a straight line whether the operating frequency of the signal source also increases. Furthermore, nonvolatility tests were also shown and one can observe in Figure 7 that the range of variation of each incremental and decremental fracmemristance is reduced when α decreases. Finally, it is worth remarking that to the best knowledge of the authors, solid-state FOMs have not been still fabricated and therefore, not only the use of emulator circuits is necessary for researching and improving future real applications [27, 28], but also FOM emulator circuits have not been reported in the literature, until today.

Data Availability

Experimental and simulation data along with source files can be obtained through a letter sent to first author, explaining their intended use.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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